An Incremental ADC Sensor Interface with Input Switch-Less Integrator Featuring 220-nV$_{RMS}$ Resolution with ±30-mV Input Range

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***Abstract*—An incremental ADC for Wheatstone CMOS stress sensor systems is described. A switched-capacitors integrator without switches toward virtual ground avoids spur signals, clock feed-through, residual offset and glitches. The circuit, fabricated in a 0.35-µm CMOS technology, consumes 42 µW at 500-kHz clock and 2.8-V supply. Low speed chopping cancels offset and limits the 1/f noise contribution. The signal-to-noise ratio with measures lasting 2^{20} periods is 114 dB at ±100 mV full-scale range. The active area is 0.32 mm^2.**

I. Introduction

1/f noise, kT/C noise and, when using ΣΔ based schemes, [1], limit cycles challenge the design of high-resolution analog-to-digital converters (ADCs) for interface sensor applications, [2]. The 1/f noise imposes large transistor and/or chopper stabilization, [3] [4]. Very high resolutions require very large sampling capacitors because of the kT/C limit. Low noise pre-amplification moderates the problem: however, gain linearity and accuracy of the preamplifier are problematic. The use of ΣΔ modulators diminishes the sampling capacitance because of the oversampling, [5] [6], but, with very low input bandwidth, accuracy can be destroyed by limit cycles.

The above concerns motivate this incremental ADC interface for label-free DNA detection where static piezo-resistive micro-cantilevers, arranged in a 4-terminal Wheatstone bridge, are used, [7]. The label-free technique enables high parallelism, which potentially allows multiple detections on the same chip with redundancy and complementary measurements. This application demands for a readout channel with very high sensitivity, low power consumption, and small area. Readout circuits for resistive sensors with performance at the state of the art are reported in [8], [5], and [7]. The solution described in [8] uses a programmable analogue front-end before a digital conversion for mismatch and offset calibration with gain correction. The achieved performance of the readout channel is of about 160 dB with a reported accuracy of 0.1%. Better results are obtained from the circuit reported in [5] that uses a cascade of a 3-stage current-feedback instrumentation amplifier and an incremental ΣΔ modulator. The scheme of reference [5] achieves 21 bit of resolution over ±40 mV input range consuming 1.35 mW and using an active area of 6 mm^2. The circuit presented in [7], specifically designed for DNA detection applications, occupies an area of 1.05 mm^2 and consumes 10 mW to achieve 15 µV of resolution.

This incremental ADC does not use pre-amplification stage, cancels offset and limits the 1/f noise contribution with double chopping technique. The scheme achieves 220-nV$_{RMS}$ resolution and input ranging from ±3 mV to ±100 mV. The circuit, fabricated in a 0.35-µm CMOS technology, has an active area of only 0.32 mm^2. Clocked at 500-kHz, the overall scheme consumes 42 µW with 2.8-V supply voltage. The gain error and gain drift only depend on matching of value and temperature coefficients of the used capacitors.

This paper is organized as follows. Section II deals with the system architecture while Section III describes the circuital details of the analog interface implementation. Section IV presents the measurement results and Section V draws some conclusions.

II. System Architecture

The very low bandwidth of the signal at the output of some sensor systems, like a Wheatstone bridge for DNA detection, enables averaging of a large number of measurements (say N), thus attenuating by $\sqrt{N}$ the kT/C requirement. This is what the first order incremental converter used in this architecture does. The scheme compensates for the 1/f noise with two methods: de-correlation obtained by current chopping, [9], and chopper stabilization, [3] [4].

The key feature of this design is a sampled data integrator in the incremental scheme without switches connected to virtual ground. This prevents virtual ground clock feed-through, residual offset and glitches. Fig. 1 shows the block diagram. The scheme uses a chopper modulation of the supply of the bridge, Φ_B, that is in phase with the clock, Φ, for a given number of clock periods and out of phase for another equal number of clock periods. Result, as better understood shortly, is an alternate positive and negative integration of input. Therefore, the system performs a double chopping: one at low frequency (de-chopped in the digital domain), the other at the clock speed.

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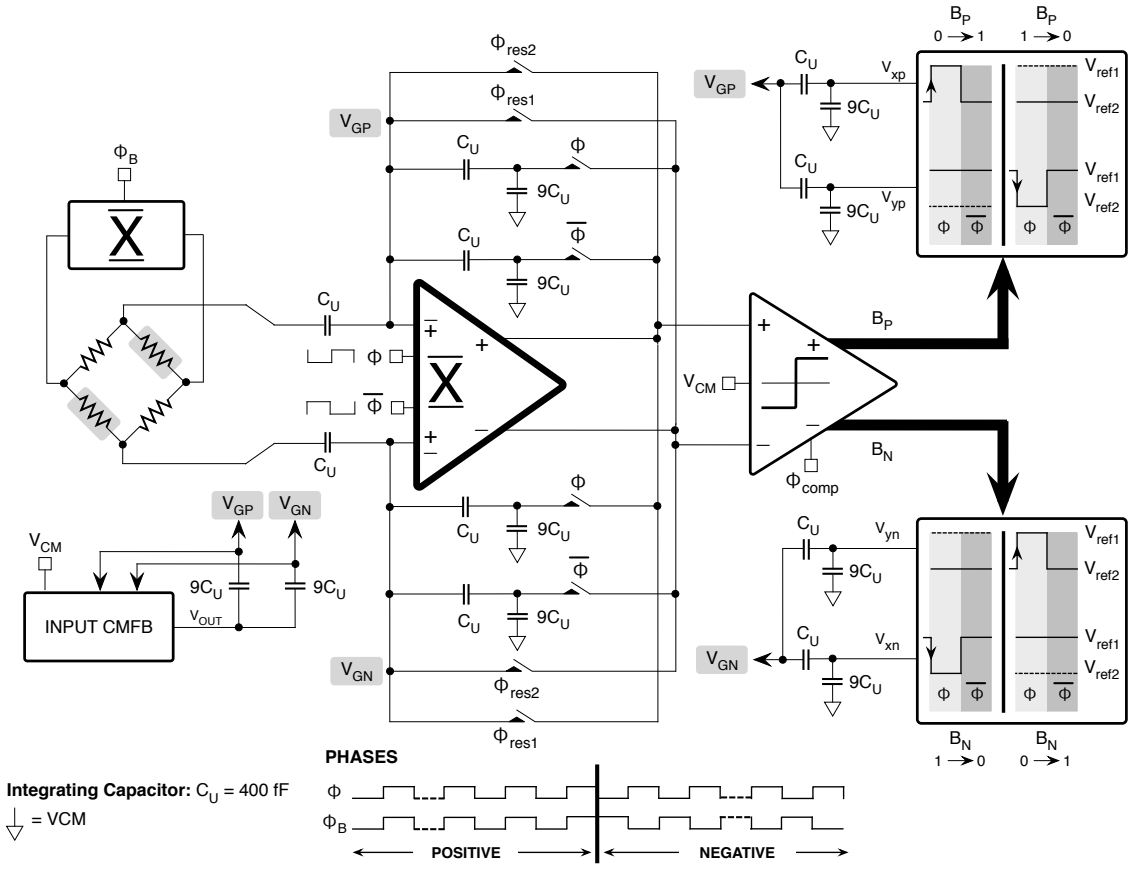

Fig. 1. Block diagram of the proposed incremental ADC interface with input switch-less integrator.

A non-conventional operational amplifier (op-amp), shown in Fig. 1, and switched capacitors give rise to the input integration. The inputs of the fully differential op-amp reverse their role of inverting and non-inverting terminal under the control of the clock. Two unity capacitors, suitably connected in feedback by switches, integrate the positive and negative charge delivered by the input capacitor during the complementary phases. The use of the $9C_U$ capacitances reduces by 10 the kT/C noise power across the integrating capacitor and attenuates the clock feed-through. The comparator determines the output bit-stream and controls the digital-to-analog converters (DACs) that operate similarly to the input stage, as shortly described.

Fig. 1 illustrates the operation of differential DACs realized without switches toward virtual ground. For each DAC there are two unity capacitors. One terminal is connected to the virtual grounds V_{GP} and V_{GN}, the other is biased to V_{ref1} (or V_{ref2}). A control bit 1 gives rise to a pulse at the right terminal of the top capacitance that goes from V_{ref1} to V_{ref2} and returns to V_{ref1} or, vice-versa, from V_{ref2} to V_{ref1} and back to V_{ref2} for the complementary DAC. Therefore, the top capacitor produces a negative injection on the positive input during Φ and, during the complementary phase, when the voltage returns to V_{ref1}, a positive reference charge into the same terminal that becomes the negative input. When the bit is 0 the top capacitor is inactive and injections with opposite sign occur because of the activity of the DACs bottom capacitors. Notice that only one switch exercises the right terminal of capacitors DAC.

The reset switches act before the measurement to cancel the memory of previous acquisitions. Since they remain open during the entire incremental measurement, there is no switching action on the virtual ground during integration.

The use of an incremental solution leads to Nyquist-rate conversion. However, since the scheme does not use S&H, the conversion result is the average of the signal in the conversion time-period. This incremental converter is a first order. It requires 2^N clock periods to generate N-bit at output. Modulators with higher order would reduce the conversion time. However, a post processing with cascade of integrators would make it difficult limiting the 1/f noise. Moreover, for low values of sampling capacitance, very large averaging periods are necessary, like the 2^{20} clock periods used in this design. Therefore, long acquisitions are necessary anyway.

The circuit uses 0.4 pF as unity capacitance. The $(kT/C)^{1/2}$ noise voltage given by 4 pF is 32 μV. Using this value in the noise calculation and accounting for an equal op-amp noise contribution, the expected root mean square (RMS) noise, averaged over 2^{20} clock periods, is equal to 166 nV.

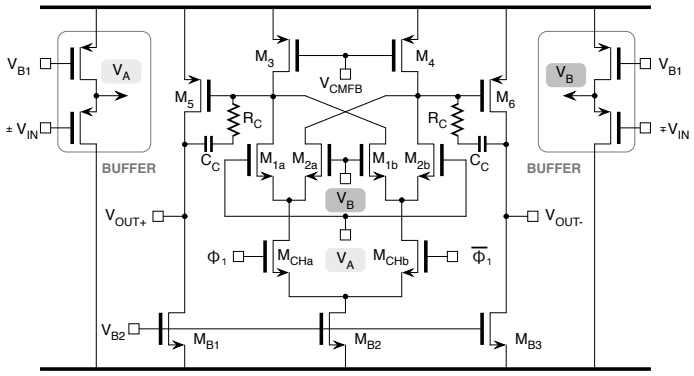

Fig. 2. Schematic diagram of the amplifier.

III. Circuit Implementation

Fig. 2 shows the schematic diagram of the op-amp. It uses two p-channel input buffers to limit the clock kickback and two input differential pairs. The clock toggles the bias current between the stages so that one operates while the other has zero current. The switching, other than inverting the role of input terminals, partially de-correlates the 1/f noise of the input pair. The second stage is a conventional inverter with active load. Voltages V_{B1} and V_{B2} are generated by a biasing circuit (not shown in the figure) while a conventional switched-capacitors common mode control acts on transistors M_3 and M_4.

Since the input terminals are floating nodes, it is necessary using reset switches at the input of the conversion cycle. The slow de-chopping in the digital processing cancels the possible offset caused by clock feed-through. A possible mismatch between capacitors produces a gain error and, in addition, a mismatch between input elements causes a common mode term rejected by the output common mode feedback. However, since the input terminals are floating during the measure, the input common mode voltage drifts and this can push the op-amp in a bad region of operation. The solution to the problem is the input common mode control of Fig. 3. A simple stage shifts the average of the input voltages; a single stage amplifier biases two $9C_U$-shifting capacitances. Voltage V_B is generated by a biasing circuit (not shown in the figure).

Fig. 4 shows the schematic diagram of the voltage comparator. It is a four input fully-differential preamplifier with a 10-dB gain and continuous time output common mode control followed by a regenerative latch, [10]. The preamplifier increases the signal level and limits possible kickback from the regenerative stage. Voltages V_{CB1} and V_{CB2} are generated by a biasing circuit, not shown.

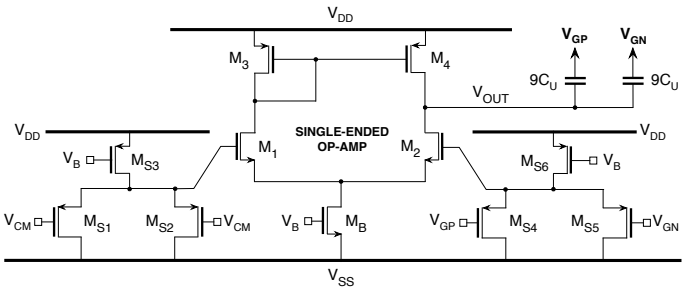

Fig. 3. Schematic diagram of the input common mode control circuit.

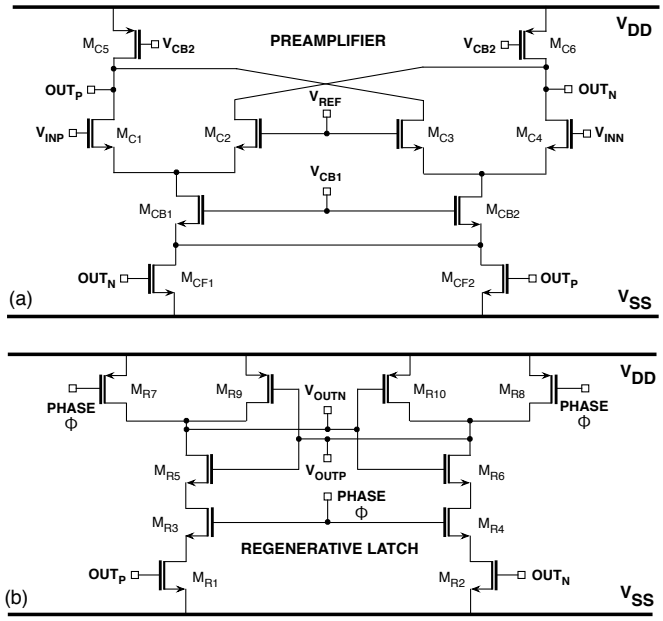

Fig. 4. Schematic diagram of the voltage comparator. a) Preamplifier. b) Regenerative latch.

IV. Measurement Results

The incremental converter has been integrated with a 4-metal 2-poly 0.35-μm CMOS technology. Fig. 5 shows the chip microphotograph with the main blocks highlighted. The active area is 0.32 mm^2. The power consumed, with 500-kHz clock and 2.8-V supply, is 42 μW.

Fig. 6 shows the measured RMS noise voltage and the achieved signal-to-noise ratio (SNR) as a function of the DAC reference voltage with 500-kHz clock frequency (f_{ck}). The slow chopping frequency is $1/4096 f_{ck}$. The measure lasts 2^{20} clock periods. The RMS of the input referred noise

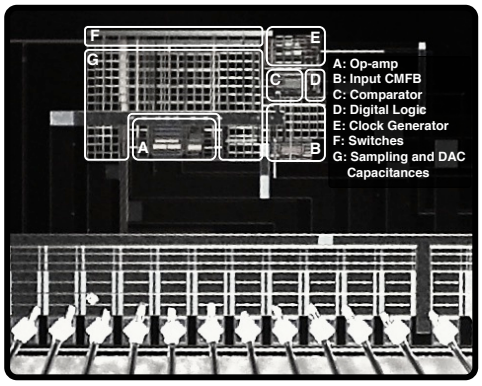

Fig. 5. Chip microphotograph.

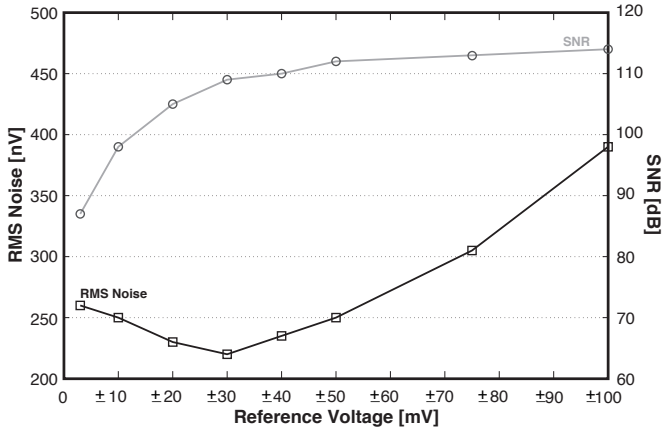

Fig. 6. Measured RMS noise voltage and SNR as a function of the DAC reference voltage.

(measured with zero input) depends on the DAC reference voltage. It varies from 260 nV to 390 nV for DAC reference voltage ranging from ±3 to ±100 mV, with a minimum of 220 nV. The SNR goes from 88 dB (14.3 effective number of bits (ENOB)@±3 mV reference voltage) to 114 dB (18.7 ENOB@±100 mV).

The value of the RMS input referred noise has been verified by repeated measurements (96) with input signal of 557.98 μV and ±30 mV DAC reference. Fig. 7, that shows the output code distribution, gives a standard deviation of 3.84 LSB@20-bit corresponding to 219 nV. This value is above the estimated kT/C noise level. The difference with respect to the estimated 166 nV is likely due to noise on reference generators and a residual 1/f noise term, as indicated by the asymmetry of the histogram, [11].

Fig. 8 shows the measured integral non-linearity (INL) of the incremental converter with ±30 mV DAC reference. The obtained INL is about ±4 LSB@20-bit.

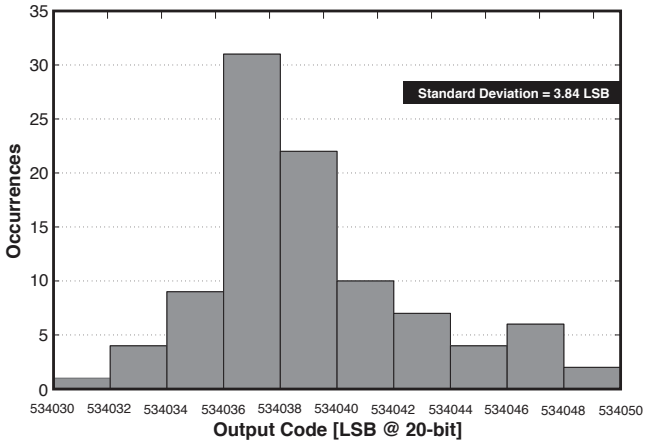

Fig. 7. Repeated measurements distribution.

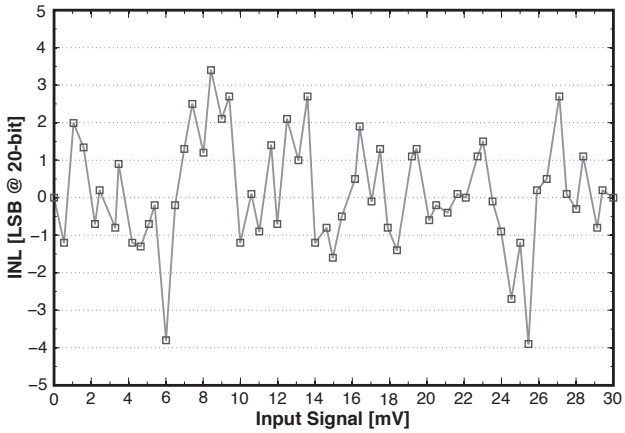

Fig. 8. Measured converter INL (positive input side).

V. Conclusions

This incremental ADC achieves 220-nV$_{RMS}$ resolution and input ranging from ±3 mV to ±100 mV. The key feature of this design is a sampled data integrator in the incremental scheme without switches connected to virtual ground. The scheme compensates for the 1/f noise and cancels the offset with two methods: de-correlation obtained by current chopping and chopper stabilization. The circuit, fabricated in a 0.35-μm CMOS technology, consumes 42 μW at 500-kHz clock and 2.8-V supply.

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