High-Order Multi-Bit Incremental Converter with Smart-DEM Algorithm

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***Abstract*—This paper describes the design method for high-order multi-bit incremental converters aiming at high resolution (> 14 bits) with Smart-DEM algorithm. Traditional 2^{nd} and 3^{rd}-order incremental ADCs use 1-bit quantizer. These structures lead to long conversion time for each sample to achieve the expected resolution and high power consumption due to the large output swing of the op-amps. Also, the fractional coefficients along the accumulation path that avoid instability degrade the performance. On the contrary, modulators employing multi-bit quantizer and DAC do not suffer from these problems. Although the mismatch of unity elements in the DAC causes non-linearity issue, this can be suppressed by Smart-DEM algorithm. Because the Smart-DEM algorithm is quite compact and easy to implement, the modulator benefits extra bits performance directly from the multi-bit DAC with affordable digital circuits overhead. In this paper several structures for incremental ADCs utilizing multi-bit quantizer are presented. The positive-and-negative DAC and the Smart-DEM algorithm are explained. With 3-bit quantizer, the simulation results show that the 2^{nd}-order incremental ADC obtains 18-bit resolution with 256 clock periods.**

I. Introduction

Sigma-Delta ($\Sigma\Delta$) analog-to-digital converters (ADCs), due to their insensitivity to circuit imperfections and ease of realization, are widely used in multimedia and telecommunication applications. However, instrumentation and measurement (I&M) applications require ADCs with high resolution, good linearity and low offset [1]. Hence, it is not suitable to apply $\Sigma\Delta$ ADC to meet those needs. On the contrary, the incremental converter, often derived from $\Sigma\Delta$ modulator, is appropriate candidate for the above requirements. Although sharing almost the same scheme with the $\Sigma\Delta$ counterparts, the incremental ADC resets the integrators periodically and provides a sample-to-sample data conversion.

The first incremental ADC was presented by Van De Plassche in 1978 [2]. Fig. 1 illustrates the block diagram of a 1st-order incremental converter. It consists of an integrator with one clock period delay, a comparator and a 1-bit DAC. The working principle is as follows: at the beginning of a new conversion cycle, the output of the integrator is reset. The input signal V_{in} can be regarded as constant because of its very low frequency. In each clock cycle, V_{in} subtracts V_{out} and the difference is accumulated on the integrator. At the end of N clock cycles, the residue voltage of the integrator is

$$V_{res} = \sum_{i=1}^{N-1} V_{in}(i) - \sum_{i=1}^{N-1} V_{out}(i) \tag{1}$$

The value of V_{res} is limited because of the stability of the feedback loop. Thus, the input signal can be estimated as below

$$V_{in} = \frac{\sum_{i=1}^{N-1} V_{out}(i)}{N-1} + \frac{V_{res}}{N-1} \tag{2}$$

The resolution of the 1st-order incremental scheme, hence, is given by

$$R_{1-ord} = log_2(N-1) \tag{3}$$

Unfortunately, the conversion efficiency of a 1st-order incremental ADC is low. Methods for increasing the resolution are augmenting the number of clock periods N and using more effective schemes with cascaded accumulators. High-order incremental ADCs, therefore, contain multiple sampled-data integrators with reset at the beginning of the conversion cycle. The key point is to increase the accumulation efficiency, maintain the stability of structure and keep V_{res} minimized, [3] [4].

An incremental converter often uses single-bit instead of multi-bit quantizer. With a single-bit quantizer, the modulator does not suffer from non-linearity resulting from mismatch of the DAC. In such case, the integrators along the accumulation path have a relatively large output swing. This may result in operational amplifiers working in slewing mode. The non-linearity of the multi-bit DAC can be compensated for with

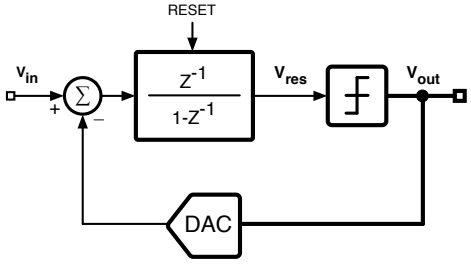

Fig. 1. 1st-order incremental ADC block diagram.

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static or dynamic calibration methods. For Sigma-Delta modulators, the well-known dynamic-element-matching (DEM) methods such as DWA [5] are possible solutions. However, these methods are not suitable for incremental converters. To our best knowledge, very few papers studied this problem. As an alternative solution the work proposed in [6] is a 2nd-order modulator with an intrinsic linear 3-bit DAC achieving 18-bit resolution without using DEM.

To maintain stability, distributed feedback or feed-forward paths are used in the modulator. Although the inaccurate feed-forward coefficients cause error along the signal path, it is just a gain factor since the input signal is almost constant. However, it is quite difficult to analyse the error due to the inaccurate feedback coefficients. This is because the feedback signal varies in time and injects signal in different locations.

In this paper, high-order incremental ADC schemes utilizing Smart-DEM algorithm are presented. In order to obtain incremental converters with high resolution, short conversion time and low-power, multiple strategies are used. These strategies include choosing structures which avoid distributed feedback injections, keeping low the swing of the integrators and employing the multi-bit quantizer compensated by Smart-DEM algorithm.

The organization of the paper is as follows: Section II proposes the structures for high-order multi-bit incremental ADCs. In Section III, the Smart-DEM algorithm and the positive-and-negative DAC are explained. Taking a 2nd-order incremental ADC as an example, Section IV shows the behavioural level simulations and the results. The conclusions are finally given in Section V.

II. Proposed Multi-Bit Incremental ADC Schemes

The above analysis gives the guidelines to design high resolution, multi-bit and low-power incremental converters as below

1) The output swing of integrators should be minimized to improve the linearity of the op-amps, as well as to reduce the number of comparators in the quantizer.
2) The number of levels of the multi-bit DAC should be minimized so as to limit the complexity of Smart-DEM algorithm.
3) There should be only one feedback path in which Smart-DEM algorithm can be effectively used.

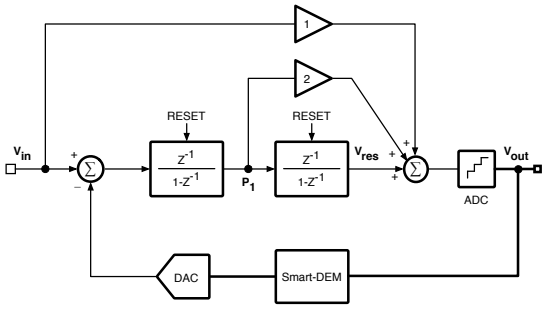

Fig. 2. A 2nd-order incremental ADC.

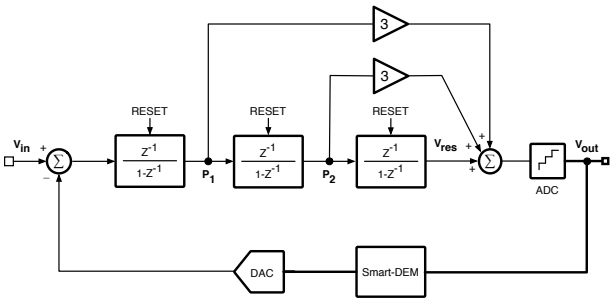

Fig. 3. A 3rd-order incremental ADC.

4) The coefficients along the accumulation path should not degrade the resolution.

The guideline 1) considers how to achieve low-power consumption of the analog circuit. 2) and 3) are used to reduce the complexity of Smart-DEM implementation, thus, optimizing the power consumption of the digital part. The guideline 4) results in easier implementation of the analog coefficients and avoids performance degradation. By adopting these guidelines, different 2nd and 3rd-order schemes are discussed in the next two subsections.

A. The 2nd-Order Architecture

Fig. 2 shows a 2nd-order incremental ADC. This modulator includes two integrators, an analog summation node with two feed-forward paths, a multi-bit ADC and a multi-bit DAC assisted by Smart-DEM block. This structure is similar to the schemes proposed in [4] and [7]. The difference is that, in [7], the suggested structure is a Sigma-Delta modulator and thus the DWA algorithm works. However, in [4], the same 2nd-order scheme is reconfigured as an incremental converter. Since the DWA algorithm is not able to compensate for the error caused by the mismatch of the DAC elements, the modulator employed 1-bit quantizer and used an extended stage to boost the performance. Here, we use a modulator with the same 2nd-order structure combined with a multi-bit quantizer. The Smart-DEM block compensates for mismatch among unity elements used in multi-bit DAC. Thus, the modulator benefits extra bit performance.

By applying the theory for incremental converters reported in [8], the maximum achievable resolution for the used 2nd-order modulator is

$$R_{2-ord} = log_2 \frac{(N-1)(N-2)}{2!} + b_q \qquad (4)$$

where N is the number of conversion cycles and b_q is the resolution of the quantizer.

B. The 3rd-Order Scheme

To further augment the conversion efficiency, a 3^{rd}-order incremental modulator is illustrated in Fig. 3. This structure resembles the 3rd-order feed-forward scheme proposed in [3]. Still, the improvement lies in the use of multi-bit quantizer instead of the simple comparator used in [3]. Although three

integrators increase the conversion efficiency, the instability problem rises. Notice that the use of multi-level quantizer (b_q >3) makes the scheme stable. On the contrary, for lower ADC resolution it is necessary to use attenuation coefficients which, however, limit the overall resolution.

Again, by applying the theory in [8], the maximum resolution for this 3rd-order modulator is

$$R_{3-ord} = log_2 \frac{(N-1)(N-2)(N-3)}{3!} + b_q \tag{5}$$

III. Smart-DEM Algorithm for High-Order Incremental ADCs

In this section, the working principles of Smart-DEM algorithm are described. Supposing an incremental converter with only one feedback path and a b_q-bit DAC, the number of unity elements is N_{dac} ($N_{dac} = 2^{b_q}$) and the mismatch for each element can be represented by $\epsilon_i (i = 1, 2, ..., N_{dac})$. Observing that the sum of the mismatch goes to zero (otherwise it could be considered as a gain factor), the following equation holds:

$$\epsilon_1 + \epsilon_2 + ... + \epsilon_{N_{dac}} = 0 \tag{6}$$

For incremental converters, the error caused by mismatch of DAC depends on the injection time. The weight of signal injected at the beginning of the conversion is larger than the weight of one injected close the end of the conversion. Let us suppose that an incremental ADC uses N clock periods to convert one sample. The total error ϵ_{tot} is then the summation of the weighted mismatches, which can be represented as

$$\epsilon_{tot} = W_1\epsilon_1 + W_2\epsilon_2 + ... + W_{N_{dac}}\epsilon_{N_{dac}} \tag{7}$$

where W_i are the weights for each mismatch $\epsilon_i (i = 1, 2, ..., N_{dac})$. Noticing that ϵ_{tot} is predictable and if it can be further controlled with a certain algorithm, the multi-bit DAC can be used directly. The key point of the Smart-DEM algorithm is that, during the data conversion, it balances the W_i, thus minimizing ϵ_{tot}. The ideal case is that, if all the weights W_i are equal, according to (7), ϵ_{tot} is equal to 0.

A. The Principle of Smart-DEM Algorithm

The basic idea of the Smart-DEM algorithm is to dynamically balance the weights of ϵ_i along the conversion of one sample. The detailed operation is described below:

1) Before the conversion, reset the weights for all the elements to zero.
2) In each clock cycle, select the unity elements with the minimum weight. If it is the last clock period, jump to Step 4.
3) Update the weight of the selected elements, then go back to Step 2.
4) Conversion finished.

The following is an example to show how this algorithm works. We use the 2nd-order structure illustrated in Fig. 2. The DAC has 6 unity elements and the time for conversion of each sample is 256 clock periods. Fig. 4 shows how the weights change inside the Smart-DEM block. Before the data conversion starts, the weight of each element is reset to 0. In clock cycle 1, the input of Smart-DEM is 4, which means 4 elements should be used. Therefore, unity elements C1, C2, C3 and C4 are chosen and the corresponding weight 254 is updated. After that, the weight array is sorted and the larger values are moved at the top of the stack. In clock cycle 2, the input for Smart-DEM is 3 and 3 elements with the minimum weight are selected (C5, C6 and C1). However, the corresponding weight of this clock period changes to 253 and it should be added to the existing weights. After sorting, the minimum weight in the array is subtracted from all weights in case of hardware overflow. This is because the word length of the weight is limited in real circuit. Finally, after 256 clock periods, the $W_i (i = 1, 2, ..., 6)$ is no more than 2 and the total effect of the mismatch is negligible.

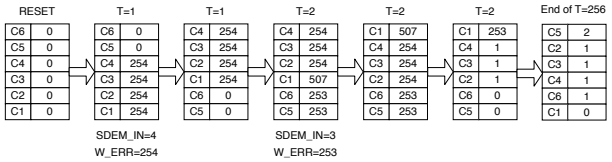

Fig. 4. The status of the weights in Smart-DEM with $V_{in} = 0.926V_{ref}$.

B. Smart-DEM for 2nd-Order and 3rd-Order ADC

This subsection discusses how to apply the Smart-DEM algorithm to different high-order incremental ADCs. The design of optimal Smart-DEM block deals with 4 main factors: the number of elements in the DAC, N_{dac}, the number of integrators, N_{ord}, along the accumulation path, the number of delays, N_{dly}, on this path, and the number of clock periods for one-sample-conversion, N. In order to reduce N_{dac}, a positive-and-negative DAC is used. It has the same function as a normal DAC but with half unity elements. This will be further discussed in the next subsection. For the 2nd-order incremental ADC shown in Fig. 2, $N_{ord} = N_{dly} = 2$. If an error from DAC enters at k-th period after the reset, the weight of this error can be calculated as

$$W_{2-ord} = N - k - 1 \tag{8}$$

However, for a 3rd-order incremental modulator, the weight for each clock cycle is a parabolic function. Take the scheme in Fig. 3 as an example. Here, $N_{ord} = N_{dly} = 3$. The weight of the error can be calculated as

$$W_{3-ord} = \frac{(N-k-1)(N-k-2)}{2!} \tag{9}$$

C. Smart-DEM with Positive-and-Negative DAC

As mentioned above, a positive-and-negative DAC is used to diminish the number of elements in the DAC. Fig. 5 (a) shows a conventional capacitive DAC with 2 elements implemented with switched-capacitors. In order to simplify this structure, Fig. 5 (b) shows a positive-and-negative DAC. The left side of the capacitor C_u is connected to positive or negative references either during phase 1 or phase 2. As specified by the table in the figure, the digital controls A_1 and

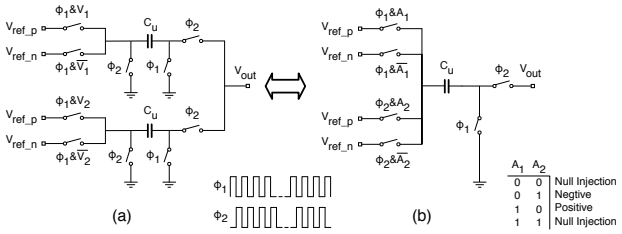

Fig. 5. The conventional DAC and positive-and-negative DAC.

A_2 can give rise to positive, negative or null injection. The use of the same capacitor makes exactly symmetric positive and negative injections. When an element represents a negative number, the mismatch weight is added to the other elements because (6) holds.

IV. Simulation Results

The described approach is valid for any architecture. Here we verify performance with the 2nd-order architecture of Fig. 2 as an example. The target resolution is 18-bit. According to (4), we choose $N = 256$ and $b_q = 3$. Behavioural level simulation results show that the output swing of both integrators is below $0.3V_{ref}$, being V_{ref} the reference voltage. In order to accommodate an overload of $\pm 20\%$, it is necessary to use 13 levels. By using the positive-and-negative DAC, the number of unity elements is 6.

Fig. 6 shows a performance comparison of the same 2^{nd}-order scheme in three different cases: mismatch in the DAC unity elements not compensated (top), compensated for with the conventional DWA method (middle), and compensated for with the Smart-DEM algorithm (bottom). The mismatch for the 6 unity elements obeys normal distribution with zero mean value and $\sigma = 2.0\%$. Such a large value is chosen in order to show the effectiveness of the proposed method. The input is a constant voltage ranging from 0 to $V_{ref} = 1V$. With this large mismatch, the maximum error with no compensation is about 1300 LSB. When using DWA, the error is not linear with a maximum of 42 LSB. The Smart-DEM is able to keep the error within ± 0.5 LSB for entire range.

Fig. 7 shows the weight accumulation of the six used elements within a single 256-period conversion. The input signal is $0.154V_{ref}$. Inset shows a detail of the last 60 clock periods. Notice that at the first clock period only one element has weight equal to 254 while the others are all equal to zero. At the end of the conversion, the weights of all the elements converge to the same level with a maximum difference of 3. This results in a negligible residual error.

V. Conclusion

Multi-bit quantization in incremental converters is possible only if the unity elements mismatch is carefully compensated for. The conventional DEM methods used for $\Sigma\Delta$ modulators are not suitable for incremental schemes. The Smart-DEM approach described in this paper shows an effective cancellation

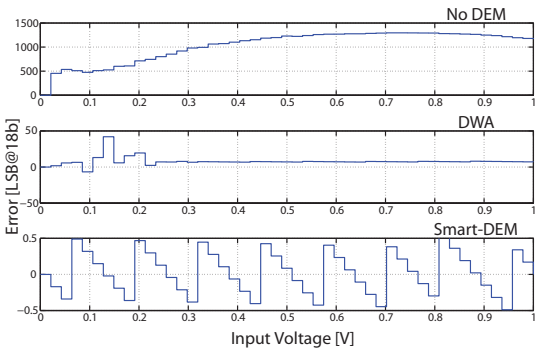

Fig. 6. Conversion error as a function of the input signal in three cases: no DEM (top), DWA (middle) and Smart-DEM (bottom).

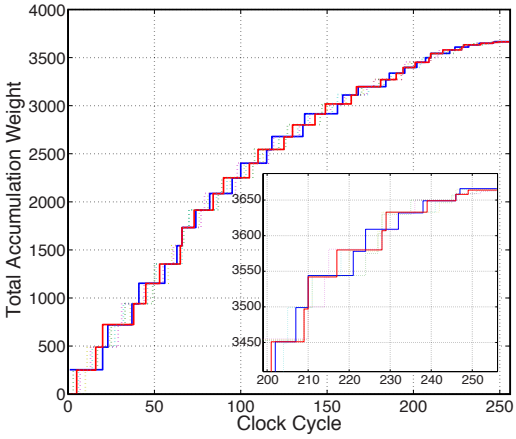

Fig. 7. Accumulation of the elements weights. Inset shows a detail of the last 60 clock periods.

for second and third-order architectures and more than 18-bit of accuracy. Extensive behavioural simulations verify the effectiveness of the approach.

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