Low-Noise Low-Offset Current-Mode Hall Sensors

Hadi Heidari, Umberto Gatti, Edoardo Bonizzoni, and Franco Maloberti
Dipartimento di Ingegneria Industriale e dell'Informazione
University of Pavia, Pavia, Italy
E-mails: hadi.heidari@unipv.it, gattiu@alice.it, edoardo.bonizzoni@unipv.it, franco.maloberti@unipv.it

***Abstract*—The performances of a current-mode Hall sensor featuring output current signals are discussed. The current-mode approach is analyzed by applying for first time to our best knowledge the spinning current technique to Hall plate working in current-mode to eliminate offset and $1/f$ noise. Among different geometries that have been studied and simulated using COMSOL Multiphysics™, cross-shaped model displayed the lowest noise and residual offset and the best sensitivity. The COMSOL results determined a behavioral model implemented in Verilog-A for simulations in the Cadence environment. Simulations results achieved in COMSOL and in Cadence environment show the potentiality, thus demonstrating the effectiveness of the approach, for a possible use of the device with remarkable performances.**

I. Introduction

Hall effect sensors have been used for various applications such as current sensing, position detecting, electronic compass and contactless switching within automotive and industrial electronics, which are fully compatible with commercial integrated circuit technologies of CMOS process, [1-3].

Signal to noise ratio (SNR) and offset are important features in Hall sensors performance evaluation. Several techniques have been developed in order to improve these characteristics. Most of them, [1-4], are based on conventional voltage-mode Hall transducers. When used in the voltage-mode, Hall sensors convert the magnetic field to be measured into an output voltage, as shown in Fig. 1(a). For many years voltage-mode Hall sensors have been absolutely dominant in most of the applications.

This paper uses a cross-shaped Hall plate in the current-mode in order to have current and not voltage as an output signal. The proposed scheme is illustrated in Fig. 1(b). A bias current is injected into two terminals of the Hall plate (A and B in this figure) and, in presence of a magnetic field, two differential output currents are available at the other two terminals. The current-mode Hall sensor has advantages when compared to its voltage-mode counterpart such as less number of terminals, easier ultimate miniaturization of the device, less parasitic effects in its high-frequency operation, no variation of the terminal potentials and so no influence of the parasitic capacitances, [1].

This paper considers several current-mode Hall effect plates modeled and evaluated with respect to noise, offset and sensitivity using 2D COMSOL Multiphysics™, [5]. The cross-shaped model emerged as the optimum plate to fit the lowest noise and residual offset and the best sensitivity. The symmetrical cross-shaped Hall plate is widely used because of its high sensitivity and immunity to alignment tolerances resulting from the fabrication process. Generally, the output offset strongly limits the DC resolution of the sensors. The use of the crossed-shaped Hall plate and of the proposed current-mode approach enables to first time at our best knowledge the use of current spinning technique, [6], in current-mode Hall sensors to reduce offset and $1/f$ noise.

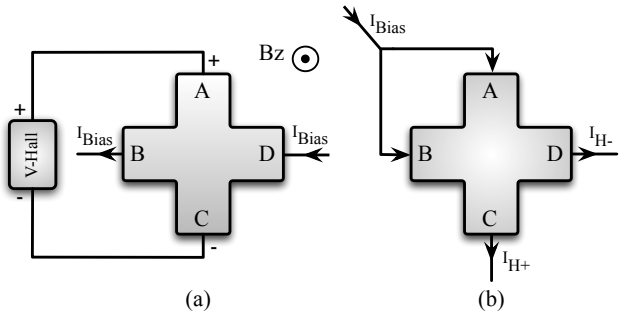

Fig. 1. (a) Hall plate operating in the voltage-mode. (b) Proposed Hall plate working in the current-mode.

This paper also analyzes the influence of the current injection and current output signals on the Hall effect sensors performances, including noise and offset, with the aid of COMSOL Multiphysics simulations. Moreover, an accurate 8-resistor network model for the cross-shaped Hall plate is described in Verilog-A and tested in a Cadence environment, [7]. Simulation results obtained in COMSOL and in Cadence environment show excellent system potentiality.

The paper is organized as follows: in the next Section the novel current-mode technique is discussed. In Section III, simulations in 2D COMSOL Multiphysics environment of the Hall plate with and without mismatch are presented. Section IV presents and discusses the model of Hall plate implemented in Verilog-A. Comparison of simulations results achieved in COMSOL and Cadence environments are also given. Section V draws some conclusions.

II. Methodology

Typically, Hall plates are used in voltage-mode. This means that the magnetic field to be measured is converted into an output voltage. The idea behind a current-mode Hall sensor is to have current and not voltage as an output signal.

The physical structure of the proposed current-mode Hall sensor is exactly the same of modern devices, with the

978-1-4673-4581-1/13/$31.00 ©2013 IEEE

same possibility of compensating for the offset caused by mismatch (current spinning). The difference is in the driving and extracting the signal.

Consider the device of Fig. 1(a); the sensor bias current I_{Bias} flows from one arm to the other in front (the symmetrical structure is for current spinning). A magnetic field B_z gives rise to the Hall voltage across the two orthogonal arms. Here, it is commonly accepted that the Hall voltage can be calculated as

$$V_H = S_I I_{Bias} B_z \tag{1}$$

where I_{Bias} is the sensor bias current, B_z the perpendicular magnetic field and S_I the current-related sensitivity. The latter is given by

$$S_I = G\frac{r_H}{qnt} \tag{2}$$

where r_H is the Hall factor, q the elementary carrier charge, n the carriers density, t the thickness of the sensor, and G a geometrical correction factor having a value in the [0, 1] interval, depending on the dimensions of the sensor.

The connection realized in the scheme of Fig. 1(b) injects the current laterally in two consecutive arms and a magnetic field causes an unbalancement of the two output currents. A difference of these output currents could be represented by an equivalent current source of a Hall current, I_{Hall}. The current-mode Hall sensor principle has been already described in [3], where it has been found that the Hall current is

$$I_{Hall} = \mu_H \frac{w}{l} I_{Bias} B_z \tag{3}$$

Here, μ_H is the Hall mobility of majority carriers, I_{Bias} is the total bias current, B_z is a normal magnetic field and $\frac{w}{l}$ is the width-to-length ratio of the plate.

This mode of operation has been extensively studied to estimate the benefit of the current-mode approach. The output currents (I_{H+}, I_{H-}) are calculated as:

$$I_{H+} = \frac{I_{Bias}}{2} + \frac{I_{Hall}}{2} \tag{4}$$

$$I_{H-} = \frac{I_{Bias}}{2} - \frac{I_{Hall}}{2} \tag{5}$$

The Hall current (I_{Hall}) is also proportional to the external magnetic field (B_z), biasing current of the Hall plate (I_{Bias}) and magnetic resistance coefficient (β). This current, for the cross-shaped Hall plate, can be expressed as:

$$I_{Hall} = \frac{\beta B_z I_{Bias}}{1 - (\beta B_z)^2} \tag{6}$$

In (6), β is magnetic resistance coefficient in presence of a magnetic field and is calculated as:

$$\beta = \frac{R_{(B_z)} - R_{(B_z=0)}}{R_{(B_z=0)} B_z} \tag{7}$$

where $R_{(B_z=0)}$ and $R_{(B_z)}$ define the Hall plate resistance in absence and presence of an external magnetic field, respectively.

TABLE I
MODEL PARAMETERS

Symbol	Value	Parameter
q [C]	$-1.602e-19$	Electron Charge
n [cm^{-3}]	$-2.6e16$	Doping
μ [cm^2/Vsec]	1200	Mobility
sigma0 [S/m]	-q*n*μ	Silicon Conductivity
R$_h$ [m^3/C]	$-1/(q*n)$	Hall Coefficient
B$_z$ [mT]	0 – 20	Magnetic Field
V$_0$ [V]	0.02	Applied Voltage
t_si [m]	$0.3e-6$	Silicon Tickness
I$_0$ [μA]	12	Input Current

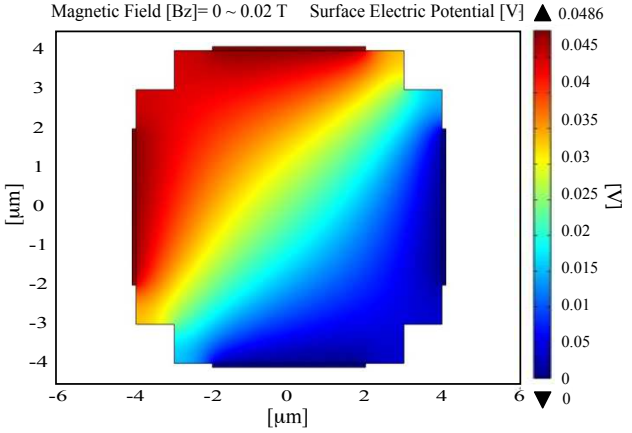

Fig. 2. COMSOL simulation.

III. SIMULATION MODEL

The current-mode technique applies to a two-dimensional model of the Hall plate simulated in COMSOL Multiphysics, [5], with parameters summarized in Table I. Fig. 2 shows the model geometry of the Hall plate: the maximum width and length is 8 μm. The figure also shows the surface electrical distribution when a magnetic field of 20 mT is applied. The simulation uses the nominal bias current of 12 μA injected in terminals A and B. The model geometry of the Hall plate has been simulated both without any mismatch and with mismatch. Results are summarized in the following sub-sections.

A. The ideal Hall plate (without mismatch)

Consider again the scheme of Fig. 1(b). Fig. 3 shows the simulated input and output currents of the Hall plate with no-mismatch. The solid line shows the input currents of A and B (equal to 6 μA) terminals while the dash-dotted and the dotted lines represent the currents at C and D terminals. These output currents increase and decrease, respectively, by changing the magnetic field within the 0 to 20 mT range. Table II summarizes the simulation results plotted in Fig. 3. The maximum differential output current is 13.3 nA for a magnetic field equal to 20 mT. These current levels are pretty

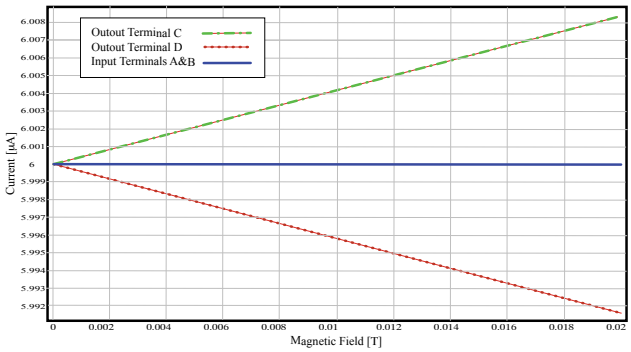

Fig. 3. Simulated input and output currents of the current-mode Hall plate.

TABLE II
SIMULATION RESULTS

Magnetic Field	Current[μA]		
B_z [T]	A+B	C	D
0	12	6	6
0.001	12	6.00033	5.99967
0.002	12	6.00067	5.99933
0.003	12	6.001	5.999
0.004	12	6.00133	5.99867
0.005	12	6.00166	5.99834
0.006	12	6.002	5.998
0.007	12	6.00233	5.99767
0.008	12	6.00266	5.99734
0.009	12	6.00299	5.99701
0.01	12	6.00333	5.99667
0.011	12	6.00366	5.99634
0.012	12	6.00399	5.99601
0.013	12	6.00432	5.99568
0.014	12	6.00466	5.99534
0.015	12	6.00499	5.99501
0.016	12	6.00532	5.99468
0.017	12	6.00565	5.99435
0.018	12	6.00599	5.99401
0.019	12	6.00632	5.99368
0.02	12	6.00665	5.99335

small, but the output signal can be increased by integrating the current signal over a given period of time.

B. Mismatched Hall plate and spinning current

Mismatch in Hall plate dimensions due to possible masks misalignment during fabrication limits accuracy and causes offset in the output signal.

As known, the spinning current technique allows strongly reducing the offset of Hall sensors, [6]. The use of the cross-shaped Hall plate and the proposed current-mode approach enables to apply the current spinning technique. The current spinning interchanges periodically the output and supply terminals of the Hall plate so that the input bias current injecting

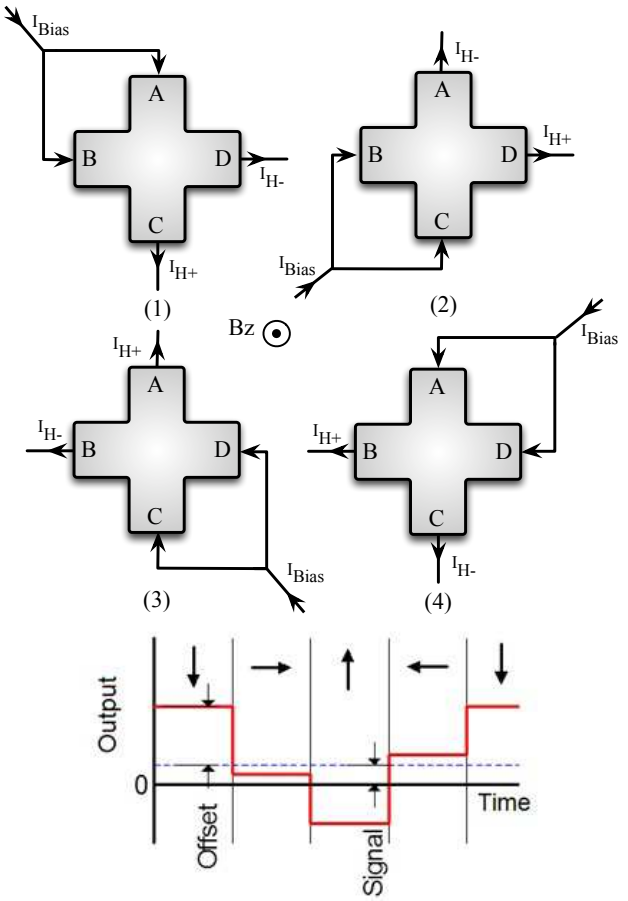

Fig. 4. Spinning current technique and output offset of Hall plate during four states.

point is rotated in each state whereas the offset appears at the output terminals. The plate is clocked with four phases and the output currents are summed.

Fig. 4 shows the four states of input and outputs for each 90 ° rotation. From the figure it can be also observed the output offset of Hall plate during the four states. After the fourth phase, it is expected that the average of the offset will be zero.

Fig. 5 shows the average of output currents of the Hall plate after spinning current as simulated in COMSOL. Simulations include a 0.01-μm mismatch in the C terminal of the Hall plate. For the spinning operation there are four phases, summarized in Table III. At the beginning, the bias current is injected into A and B terminals (phase 1). During phase 2, after 90 ° rotation, the bias current is injected into B and C terminals and so on for other phases. The used spinning frequency is 1 MHz.

From Fig. 5 it can be noted that, at the end of complete spinning and average of four phases, the offset for zero magnetic field is eliminated. When increasing the magnetic field from 0 to 20 mT, the positive output (I_{H+}) rises and the

TABLE III
FOUR PHASES FOR SPINNING CURRENT METHOD

Current	Phase1	Phase2	Phase3	Phase4
I_B	A,B	B,C	C,D	D,A
I_{H-}	D	A	B	C
I_{H+}	C	D	A	B

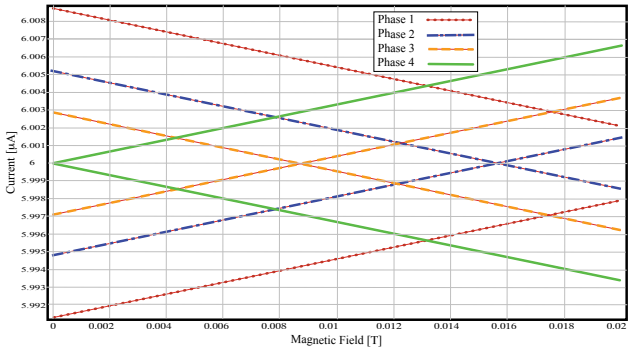

Fig. 5. Simulated average output currents (I_{H+} and I_{H-}) of current-mode Hall sensor plate with mismatch after spinning current method.

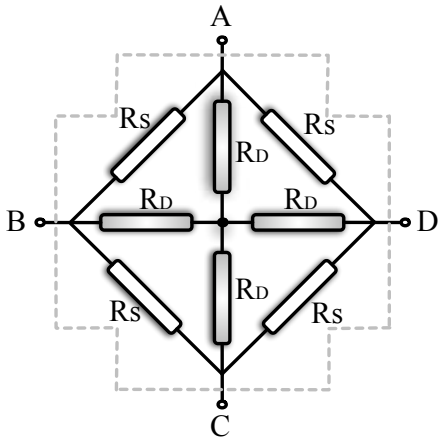

Fig. 6. The model implemented in Verilog-A using eight resistors.

negative output (I_{H-}) decreases.

IV. VERILOG-A MODEL AND SIMULATIONS COMPARISON

The Hall plate has been modeled and described using the Verilog-A language so that it can be simulated in the Cadence environment as well, [7].

Fig. 6 shows the Hall plate model. It includes four electrical terminals (A, B, C and D) and eight resistors (four side resistors, R_S, and four diagonal resistors, R_D). The values of these resistors is controlled by three parameters: the external magnetic field, the initial value of resistors, R_0, and the magnetic resistance coefficient, β. The extraction of parameters from device simulations is as follows. The initial value of resistors, R_0, is obtained in two steps. First step consists of grounding terminals C and D and applying 12 μA to terminals A and B. In the second step, terminals B and D are grounded and the current is applied to terminals A and C. The magnetic resistance coefficient, β, is defined as the average of initial values of resistors, R_0, in presence and absence of the magnetic field.

TABLE IV
COMPARISON BETWEEN THE SIMULATIONS OF THE HALL PLATE IN COMSOL AND VERILOG-A

Magnetic Field	COMSOL		VERILOG-A	
B_z[mT]	I_D[μA]	I_C[μA]	I_D[μA]	I_C[μA]
0	6	6	6	6
10	6.0033	5.99667	6.003373	5.996627
20	6.00665	5.99335	6.006746	5.993254

In order to show the correctness and accuracy of this model, the simulation results have been compared with the ones achieved with the COMSOL model, as summarized in Table IV. I_C and I_D stand for currents of C and D terminals, respectively. The results are in excellent agreement and the difference is less than 0.1%.

The simulations have been performed with 12 μA input bias current (injected in terminals A and B) while the magnetic field has been considered from 0 to 20 mT.

V. CONCLUSION

The study shows the effectiveness of a current-mode Hall sensor. The cross-shaped model has been simulated at the first using COMSOL Multiphysics and after that it has been modeled with an equivalent circuit using Verilog-A for behavioral simulations in the Cadence environment. Simulation and modeling results revealed that the proposed technique enables superior performance of magnetic field sensitivity, in terms of signal to noise ratio and sensitivity compared to the voltage-mode Hall sensors.

As future work it will be continued the analysis and the design of a complete Hall sensor microsystems, readout circuits, all using a conventional CMOS technology.

REFERENCES

[1] R. S. Popovic, *Hall Effect Devices*, 2nd ed. Bristol, U.K.: Inst. Physics Publishing, 2004.
[2] M. Pastre, M. Kayal, H. Blanchardl, "A Hall Sensor Analog Front End for Current Measurement with Continuous Gain Calibration", *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 242-243, 596, February 2005.
[3] A. Ajbl, M. Pastre and M. Kayal, "A Current-Mode Back-End for a Sensor Microsystem", *IEEE New Circuits and Systems Conference (NEWCAS)*, pp. 466-469, June 2011.
[4] G. Boero, D. Memierre, P.-.A. Besse, R.S. Popovic, "Micro-Hall devices: performance, technologies and applications", *Sensors and Actuators A*, no. 106, pp. 314-320, 2003.
[5] R. W. Pryor, *Multiphysics Modeling Using COMSOL: A First Principles Approach*. Jones and Bartlett Publishers, 2009.
[6] A. Bilotti, G. Monreal, and R. Vig, "Monolithic Magnetic Hall Sensor Using Dynamic Quadrature Offset Cancellation", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 829-836, June 1997.
[7] K. Kundert and O. Zinke, *The Designer's Guide to Verilog-AMS*. Boston: Kluwert Academic Publishers, 2004.