Single Op-Amp Algorithmic Converter and its Offset and Mismatch Compensation

Yao Liu and Franco Maloberti

University of Pavia
Dipartimento di Ingegneria Industriale e dell'Informazione
Via Ferrata, 1 - 27100 Pavia - ITALY
E-mail: yao.liu01@ateneopv.it, franco.maloberti@unipv.it

***Abstract*—This paper studies features and limits of an algorithmic ADC implemented with a single operational amplifier. Since the technique can be profitable when the resolution reaches more than 12-bit compared with SAR algorithm, it is necessary to ensure proper specification of active and passive elements or to compensate for these limits. It is shown that reconfigurability of the architecture allows measuring offset and capacitor mismatch for a background or a foreground calibration.**

I. Introduction

Algorithmic converters [1] are attractive solutions because they achieve high resolution with a number of clock periods comparable with the number of bits. They are similar to the SAR converters but an active multiplication of the signal every clock period keeps the input of the quantizer (typically a simple comparator or a flash) at a suitable large level. Normal architectures use a multiplication by 2 of the signal around the feedback loop. The input injected at the beginning of the conversion cycle is enhanced together with the signal of a DAC injected under the control of a DAC and a logic block.

The limits to the practical implementation come from the error caused by the accuracy of the multiplying factor and, in case of multi-level DAC the mismatch between the unity elements. The use of operational amplifiers implies reduction of performance caused by finite gain, offset and limited speed. Passive components are normally supposed with equal value. The matching accuracy, which must be better than the inverse of the digital dynamic range of the data converter, depends on the area of the element. Typical processes and reasonable sizes ensure accuracy between 2^{-10} to 2^{-12} range.

Achieving resolutions of more than 12-bit imposes efforts in the active devices design and corrections of technological inaccuracy. Indeed, experimental results of a previous published solution [2] showed that it is possible to achieve 12-bit resolution relying on the accuracy normally granted by available technology.

Aiming at more aggressive performance, this paper analyses limits of an effective ADC algorithm and proposes alternative solutions to overcome existing limits with digital calibration and mismatch compensation.

Next section recall the algorithmic architecture and the possible combination with the incremental method. Section III analyses the limits caused by the use of real elements, then methods for compensating for those limits for getting more than 14-bit are described.

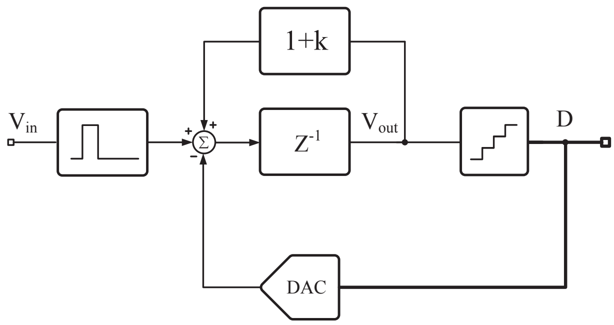

Fig. 1. Conceptual block diagram of algorithmic converter. The quantizer can be a simple comparator or a multi-bit scheme.

II. Algorithmic Architectures

Fig. 1 shows the conceptual scheme of an algorithmic converter. The input signal enters a loop at the beginning of the conversion cycle. The use of active devices multiplies the signal by a factor $m = (1+k)$ every clock period while $\pm V_{ref}$ enters the loop under the control of a comparator. The control loop keeps limited the amplitude of the output voltage V_{out}. Therefore, the following equation can be derived

$$V_{out}(n) = V_{in}m^n - \sum_{i=0}^{n-1} D(n-1-i)V_{ref}m^{n-1-i} \quad (1)$$

where, for single bit, $D(i)$ is ± 1 depending on the output of the comparator at the corresponding clock period. $D(n-1)$ is the quantization of V_{in} in the reset clock period.

The sequence of $D(i)$ is the conversion of the input voltage expressed in an m-based numbering system. If $m = 2$ the digital result is a binary code.

Possible variants to the basic algorithm are the use of a multi-level quantizer and the pre-conversion of the input with another conversion method which generates a residual (the incremental, for instance) and the refinement of the resolution by using the algorithmic method. The latter case is used in [2]: the algorithmic architecture is configured as a first order

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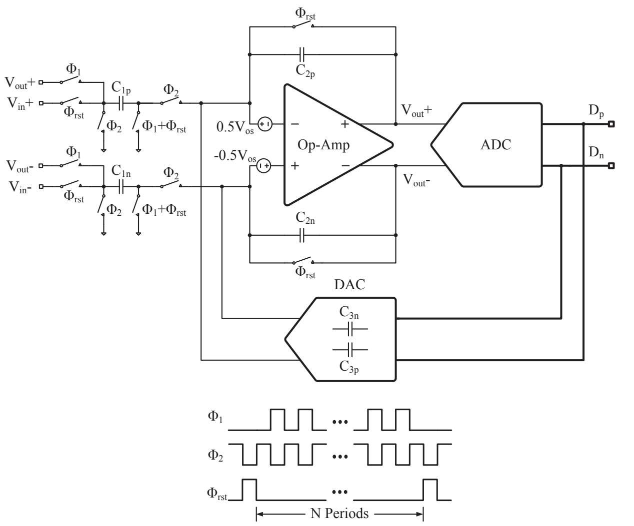

Fig. 2. Possible circuit implementation of a fully-differential algorithmic converter. The DAC establishes a C_3 load from virtual grounds to ground.

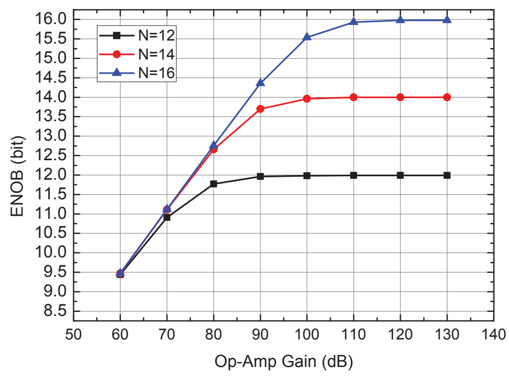

Fig. 3. Equivalent number of bit versus the finite gain of the op–amp used in an algorithmic converter.

incremental and after a number of accumulation of the input, the scheme becomes algorithmic. The result is that the number of bit determined in the preliminary phase increases the final resolution.

There are many possible schemes which realize the multiplication by m. One [1] uses a loop with two amplifiers; another follows the scheme of Fig. 1 with a positive feedback injecting k times the output at the input every conversion period. Obviously the second solution is more power and area effective as it uses only one active element.

III. Limitations

The implementation limits make the algorithmic method not very attractive. The SAR scheme achieves 10 or more bit without requiring signal amplification. This makes the method superior as far as the power consumption is concerned. For resolution of 14-bit or more, the SAR technique becomes problematic and the use of schemes with active functions becomes almost indispensable.

In order to analyse the limits we refer to the possible circuit implementation shown in Fig. 2. It is a fully differential scheme with a single op-amp and a multi-bit quantizer with a charge-generator DAC. Capacitor C_1 (and its complementary counterpart) samples the input during the reset phase. Then it injects its charge into C_2 before starting the conversion algorithm. The same switched capacitor structure C_1 amplifies the output by $m = (C_1 + C_2)/C_2$ and the DAC closes the feedback loop with an equivalent capacitance C_3 which loads the differential virtual grounds. Two differential voltage generators model the op-amp offset. The finite gain of the op-amp is A_0.

Let us consider the limits of finite gain before. The charge conservation during each conversion period is

$$\begin{aligned} V_{out}(n)(1+\frac{1}{A_0}) =& V_{out}(n-1)(1+\frac{1}{A_0})C_2 \\ &+ V_{out}(n-1)C_1 - \frac{V_{out}(n)}{A_0}C_1 \\ &+ D(n-1)V_{ref}C_3 - \frac{V_{out}(n)}{A_0}C_3 \end{aligned} \tag{2}$$

leading to

$$V_{out}(n) = \frac{a_2 V_{out}(n-1) + D(n-1)V_{ref}}{a_1} \tag{3}$$

where

$$\begin{aligned} a_1 =& \frac{C_1}{A_0} + (1+\frac{1}{A_0})C_2 + \frac{C_3}{A_0} \\ a_2 =& C_1 + (1+\frac{1}{A_0})C_2 \end{aligned} \tag{4}$$

It is evident that for different input amplitudes the digital data and the feedback give rise to a sequence of output amplitudes unrelated to the input. The result is a non linear overall error whose extent is large with low finite gains. Since estimating the effect is difficult, we used the above equation in a behavioural model to determine errors as shown in Fig. 3. The result is that a given target resolution determines a minimum finite gain. With our best knowledge, it is almost impossible to correct with digital methods the limit caused by the finite gain of the op-amp. If the loss of 0.5-bit is admitted, a 16-bit converter requires $100\,dB$ finite gain.

The number of bits of the quantizer augments the resolution of a converter without increasing the number of clock periods. However, the mismatch between unity elements used in the DAC limits the linearity and adds an error whose effect is equivalent to noise. A viable solution is to employ a three-level DAC. That is because with fully differential implementations, it is possible to ensure intrinsic symmetrical responses. The three-level DAC grants an extra bit of resolution at the expense of two comparators in the flash. However, a three-level DAC leads to imperceptible nonlinearity because of possible

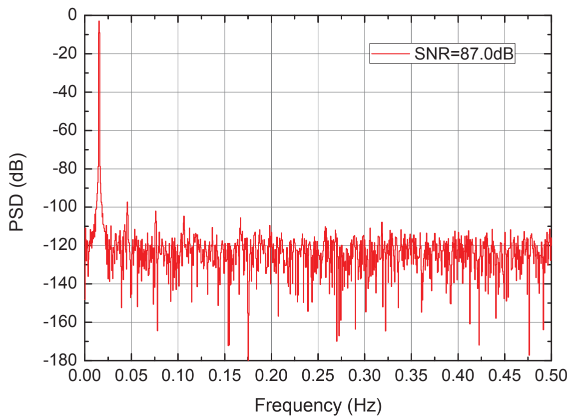

Fig. 4. Spectrum of an algorithmic converter with a 3-level quantizer.

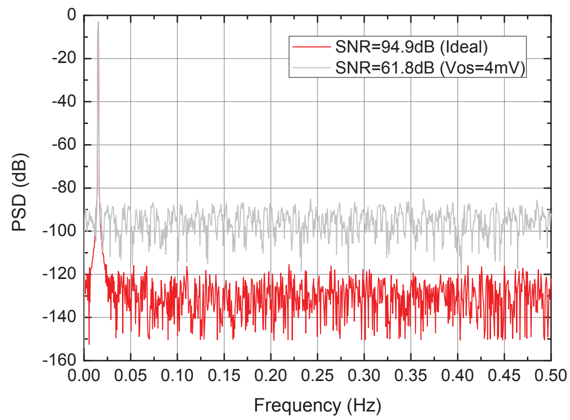

Fig. 5. Output spectrum with zero offset and 4 mV offset, showing an increase of the noise floor.

different widths of the quantization intervals representing the three logic levels. Simulation results show minor harmonic terms as outlined in the output spectrum of Fig. 4 (thresholds at $\pm 0.5 V_{ref}$). The tones are at around $-100\, dB_{FS}$, denoting a limited distortion contribution normally below common specifications.

The offset of the operational amplifier causes a shift in the injection of the signals returning back from the op-amp output and the one determined by the DAC. Accounting for the offset limit (and supposing the gain of op-amp is very large) the charge conservation equation leads to

$$\begin{aligned} [V_{out}(n) - V_{os}]\, C_2 = & [V_{out}(n-1) - V_{os}]\, C_2 + \\ & [V_{out}(n-1) + V_{os}]\, C_1 + \\ & [-D(n-1)V_{ref} + V_{os}]\, C_3 \end{aligned} \tag{5}$$

supposing $C_1 = C_2 = C_3$ it results

$$V_{out}(n) = 2V_{out}(n-1) - D(n-1)V_{ref} + 2V_{os} \tag{6}$$

Notice that there are two consequences related to the limit caused by offset. Looking from the DAC output point of view, offset corresponds to a shift of the input by $V_{os}(1 + \frac{C_1 + C_3}{C_2})$, which is equivalent to a corresponding input referred offset. The situation is different when looking at the output multiplication effect. Indeed, since the circuit achieves the multiplication by adding a replica of the output voltage V_{out}, the consequence of offset is to alter the multiplication factor. In the special case that the output equals to the minus offset, the multiplication reduces to 1, and in general is,

$$m = 1 + \frac{V_{out} + V_{os}}{V_{out}} \tag{7}$$

which changes in an unpredictable, pseudo-random manner, depending on the sequence the output voltage.

The use of the above equations to build a behavioural model verifies expected result. The output shows an offset and worsening of the equivalent number of bit because of a pseudo-white noise. Fig. 5 compares spectra with a $-3\, dB_{FS}$ input sine wave and zero or $4\, mV$ offset. The expected full scale SNR of the converter is $98\, dB$. The circuit uses two level quantizer with $V_{ref} = \pm 1V$. Result show that just $4\, mV$ degrade the performance by $33.1\, dB$ corresponding to a loss of 5.5-bit.

Fig. 6 plots resolution versus offset with expected 16 and 18-bit and $V_{ref} = \pm 1V$. The loss strongly depends on sine wave amplitude and frequency. However, $0.85\, mV$ and $0.37\, mV$ offset causes a loss of 1 bit for the two foreseen resolutions. The result shows that in order to ensure high resolution, the essential range of offset should be sub $1\, mV$.

Another important limit is given by the error caused by capacitor mismatch. Even if it is possible to limit the error, the technique such as the one proposed in [3] works well until 12-bit. Mismatch determines the accuracy of used base of numbering system, typically 2 when C_1 is chosen nominally equal to C_2. Moreover, the mismatch between capacitors C_1

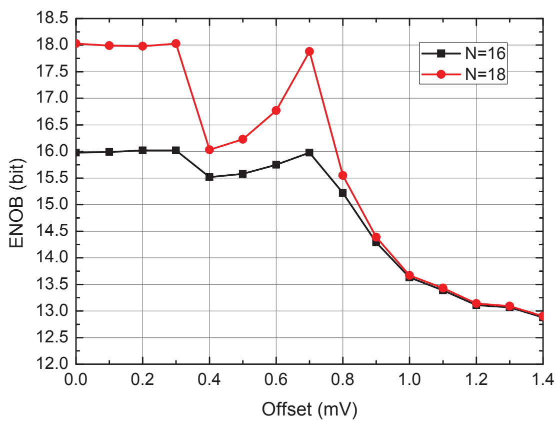

Fig. 6. Equivalent number of bit at output of a 16-bit an 18-bit algorithmic cover for different offset values.

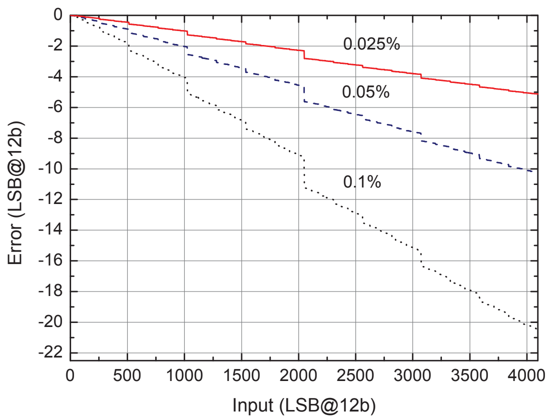

Fig. 7. Error caused by capacitor mismatch for a 12-bit ADC.

and C_2 gives rise to gain error. The difference between the effective and the expected multiplication factor causes an error which increases with the code. Fig. 7 shows the error for a 12-bit algorithmic converter with mismatches by 0.1%, 0.05% and 0.025%. Result shows a gain error and a non linear error whose maximum occurs at the mid-scale. In order to constrain the DNL below 1 LSB, a matching accuracy about $1/2^N$ is necessary, where N is the number of bit of the converter. Since with modern technologies it is possible to get 1-σ matching accuracy in the order of 0.05%, designing converters more than 10-12 bit requires actions capable to correct the mismatch limit.

IV. Error Correction

The correction of static errors in data converters can be done in the background or the foreground [5]. Here we suppose to measure errors using a foreground approach. It is possible to extend the method to background by interleaving the foreground method with normal operation.

The previous sections outlined two key limits: offset of the op-amp and mismatch between C_1 and C_2. In order to achieve good resolution, the measurement of these non-ideal factors is necessary. Notice that the scheme of Fig. 2 can be reconfigured as a first order incremental converter. After the reset of the capacitor in feedback across the op-amp, it accumulates the input signal for a given number of clock periods, say $N = 2^r$. The incremental algorithm uses only the DAC feedback. Neglecting mismatches, the final output of op-amp is

$$V_{out}(N) = NV_{in} - \sum_{i=1}^{N} V_{ref} D(i) \tag{8}$$

where $D(i)$ is ± 1, denotes the sign of $V_{out}(i)$ at the i-th clock period. The use of a large number of clock periods N measures the quantity under calibration with an r-bit resolution.

The use of the scheme of Fig. 2 in the incremental converter mode enables us to measure offset and mismatch by the following configurations:

- Measure of offset: disable SC structure with C_1. According to (8) the digital accumulation at output determines the offset. The accuracy of the measure is within the matching between the capacitors C_2 and C_3.
- Measure of mismatch between C_1 and C_2: inject a fraction α of reference voltage with SC structure C_1 and then disable it (case a). Repeat the measure with the role of C_1 and C_2 reversed and same fraction α of reference at input (case b).

After N clock periods the digital outputs in the two cases provide the following measures

$$Y_a = (\alpha V_{ref} + V_{os}) C_1 / C_3; \tag{9}$$

and

$$Y_b = (\alpha V_{ref} + V_{os}) C_2 / C_3; \tag{10}$$

with r bit of accuracy. The ratio between Y_a and Y_b determines the mismatch.

The measure of offset and mismatch can be done by a specific calibration cycle at the power-on or during inactivity periods (foreground calibration). Alternatively, it is possible to use an extra clock period per conversion and use that clock period with the incremental configuration (background calibration). In the latter case a calibration supplementary capacitor, which is inserted during the extra phase, should be employed.

The measure of offset enables its correction in the analog domain with different methods. For instance, it is possible to properly shift reference voltages or to suitably correct offset by an extra op-amp input pair. The correction of mismatch can be done by digital processing that transforms the measured result into binary.

V. Conclusions

The algorithmic converter is a good solution for achieving resolution in the 12+ bit range without the need of of very sensitive comparators as the SAR needs. The use of op-amps, however, must face finite gain, offset and mismatch between passive elements. This study outlines the specifications of various design parameters and provides useful hints for analog and digital correction to be implemented in the background or the foreground mode of operation.

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