A 2+1 Multi-Bit Incremental Architecture Using Smart-DEM Algorithm

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***Abstract*—This paper describes a multi-bit third-order incremental analog-to-digital (ADC) architecture and design considerations to achieve 18-bit resolution. The architecture uses multi-bit quantization in order to increase resolution and reduce the output swing of op-amps. The non-linearity due to the mismatch of unity elements of multi-bit DAC is properly compensated for with Smart-DEM algorithm. This 2+1 incremental architecture achieves 18-bit resolution with a 3-bit quantizer. Simulation results verify the target resolution achieved with 61 clock periods despite a large unity element mismatch ($3\sigma = 0.5\%$).**

I. Introduction

Incremental ADCs are widely used in instrumentations and sensors applications, such as readout of bridge transducers and biomedical acquisition systems [1][2]. The advantages of incremental ADCs are good linearity, high resolution, low offset and low power dissipation. Although sharing the same structures of ΣΔ modulators (ΣΔMs), incremental ADCs reset the output of integrators every N clock periods and provide a sample-to-sample conversion. They can be, hence, classified as Nyquist-rate data converters.

Incremental ADC comes from the combination of a ΣΔM and a dual-slope ADC [3]. Fig. 1 shows the block diagram of a first-order incremental ADC. It consists of a delayed-integrator, a comparator and a 2-level DAC. The operation principle is as below: when a new conversion cycle starts, the output of integrator V_{res} is reset. Since the frequency of the input signal of incremental ADCs is usually low, V_{in} can be regarded as constant. In each clock period, V_{in} subtracts V_{out} (analog version of D_{out}) and the difference is accumulated by the delayed-integrator. At the end of N clock cycles, the residue voltage at the output of integrator is

$$V_{res} = \sum_{i=1}^{N-1} V_{in}(i) - \sum_{i=1}^{N-1} D_{out}(i)V_{ref} \tag{1}$$

Due to the stability of the feedback loop, the voltage of V_{res} is limited, namely $-V_{ref} < V_{res} < V_{ref}$, where $\pm V_{ref}$ are the reference voltages. The input signal V_{in} can be, hence, represented as

$$V_{in} = \frac{\sum_{i=1}^{N-1} D_{out}(i)V_{ref}}{N-1} + \frac{V_{res}}{N-1} \tag{2}$$

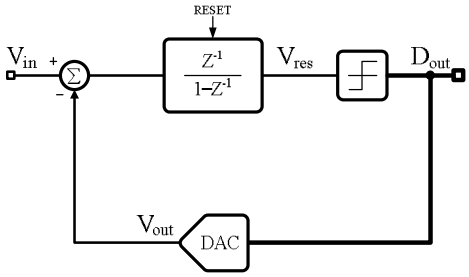

Fig. 1. First-order incremental ADC block diagram.

and the resolution of first-order incremental ADC is given by

$$R_{1ord} = log_2(N-1) \tag{3}$$

However, the conversion efficiency of first-order incremental scheme is low. Possible methods to boost the resolution are: 1) augmenting the number of clock periods, N; 2) cascading integrators along the accumulation path, thus incrementing the modulator order; 3) adding extra stages or reconfiguring the scheme to minimize the residue voltage V_{res}, [4][5].

Typically, the quantizer used in incremental ADCs is a 2-level comparator. This ensures intrinsic linearity in the feedback DAC. However, the output swing of integrators is large and may result in op-amps working in slewing mode. When the order of the scheme, L, is larger than 2, stability of the loop demands for the use of fractional coefficients along the accumulation path, which degrades the conversion efficiency. On the contrary, incremental ADCs that use multi-bit quantizer and multi-level feedback DAC do not suffer from aforementioned problems. Nonetheless, the non-linearity of multi-bit DAC in incremental ADCs needs to be properly compensated for. For ΣΔMs, static or dynamic calibrations such as dynamic-element-matching (DEM) are effective ways to compensated for non-linearity of DAC. However, those methods are not suitable for incremental ADCs. To our best knowledge, very few papers studied this problem. An alternative solution is to use a 3-bit intrinsic linear DAC without the assistance of DEM, [6]. Recently, a Smart-DEM algorithm suitable for high-order multi-bit incremental ADCs has been proposed and verified

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on silicon in [7]. That Smart-DEM assisted 3-bit second-order modulator improves the signal-to-noise ratio (SNR) of about 20 dB with respect to the case of no DEM assistance.

This paper presents a 2+1 multi-bit incremental converter made by a cascade of a multi-bit second order and multi-bit first order scheme. The multi-level DAC mismatch is compensated for with an extension of the Smart-DEM algorithm proposed in [7] for this third-order solution. The scheme achieves 18-bit resolution while using only 61 clock periods and it is able to tolerate even large unity element mismatch ($3\sigma = 0.5\%$).

II. Proposed Multi-Bit Incremental Architecture

A. Second-Order Multi-Bit Architecture

Fig. 2 illustrates a second-order incremental ADC [7]. It is the cascade of two sampled-data integrators (one without delay, the other with delay) with digital feed-forwards. The quantization step of each ADC is $V_{FS}/8$, where V_{FS} is the full-scale voltage. For such a second-order modulator, the maximum achievable resolution is

$$R_{2ord} = log_2 \frac{N(N-1)}{2!} + b_q \tag{4}$$

where N is the number of clock cycles per sample and b_q is the resolution of quantizer. With $N = 256$ and $b_q = 3$, R_{2ord} is equal to 17.99 bit. The used digital feed-forward paths limit the swing at the output of the op-amps. Thus, ADC2 and ADC3 need only 4 comparators. The second-order Smart-DEM block processes the modulator output to properly select the unity elements to be used in the multi-level DAC. The scheme ensures stability and limits the integrator swings below $0.4V_{ref}$. Moreover, the use of digital feed-forwards avoids employing an analog adder before the quantizer. This is not a limit because the converter is Nyquist rate and does not exploit oversampling to have noise shaping.

B. Third-Order Multi-Bit Incremental Scheme

Aiming at same resolution with a reduced number of clock periods, the 2+1 incremental architecture illustrated in Fig. 3 is proposed. This third-order architecture contains two stages.

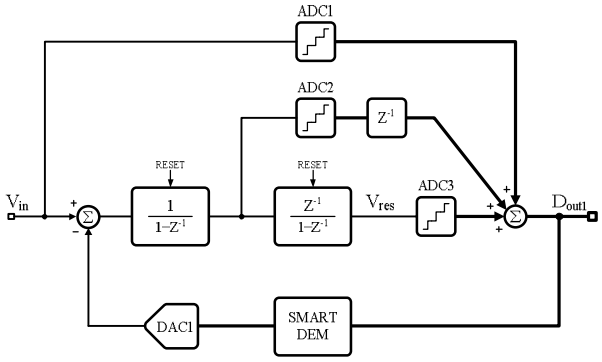

Fig. 2. Second-order incremental ADC block diagram.

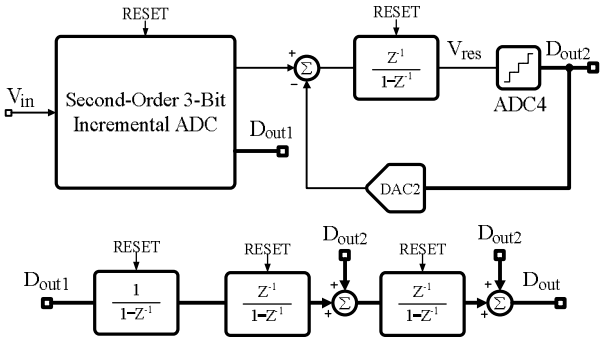

Fig. 3. Proposed third-order incremental architecture block diagram.

The first stage is scheme of Fig. 2, the second stage is a first-order scheme. This architecture operates like the extended-range solution, [5]. The extended scheme samples the residual of the second order incremental at the end of the conversion cycle and, with an extra converter, increases the resolution. The sampling of the residual, however, is a critical operation because the required accuracy is the full scale voltage divided by 2^{N_1}, where N_1 is the number of bits at the output of the second order section. Since this solution is third order like the extended resolution is $(N-2)/3$, as specified below. A possible limit comes from the inaccuracy of the gain factor of the second stage but this, as verified with simulations, is irrelevant for the level of matching accuracies of modern technologies.

The 3-bit DAC of the second stage has only 5-level. The digital output of the modulator D_{out} is the combination of the outputs as Fig. 3 shows. The resolution is estimated as [8]

$$R_{3ord} = log_2 \frac{N(N-1)(N-2)}{3!} + b_q \tag{5}$$

With $N = 61$ and $b_q = 3$, the expected resolution is 18.14 bit. Behavioral simulations show that the swings of the three integrators are $0.4V_{ref}$, $0.4V_{ref}$, and $0.5V_{ref}$, respectively. The swings of DAC1 and DAC2 are $1.5V_{ref}$ and $0.5V_{ref}$. The number of levels of DAC1 is 13 because of its swing 50% larger than V_{ref}. Its implementation requires, hence, 12 unity elements. As mentioned, DAC2 has only 5 levels, thus needing only 4 unity elements. Notice that the output is a triple accumulation of the input but the stability is ensured at the block level.

III. Design Considerations

A. kT/C Noise Limitation

For high resolution incremental ADCs, the kT/C noise is a key limitation and has to be carefully investigated. In a single-ended switched capacitor (SC) implementation of the scheme of Fig. 3, in each clock cycle, the noise injected from the input of the modulator is $2kT/C_S$, where C_S is the sampling capacitance. At the end of the N-th clock period, the total noise accumulated at V_{res} node is

$$v_{n,tot}^2 = \frac{2kT}{C_s} \sum_{i=1}^{N} \left[\frac{(N-i)(N-i-1)}{2} \right]^2 \tag{6}$$

Therefore, the input referred noise is

$$v_{n,in}^2 = \frac{v_{n,tot}^2}{G^2} \tag{7}$$

where G is the gain of the input signal that is $N(N-1)(N-2)/3!$. In order to achieve R_{3ord} resolution, the root-mean-square (RMS) value of the input referred noise should be less than half of V_{LSB}, which gives rise to

$$C_S > \frac{8kT}{V_{LSB}^2};\ V_{LSB} = \frac{V_{FS}}{2^{R_{3ord}}} \tag{8}$$

When considering $N = 61$, $V_{FS} = 3.3$ V and $R_{3ord} = 18.14$, according to (8), the minimum value of the input sampling capacitance is 6.27 pF. For a standard CMOS technology (e.g. 0.18-μm), the typical 3σ matching accuracy of MIM capacitors is normally below 1.5% and the specific capacitance per unit area is 2 fF/μm^2. However, to keep some margin when considering parasitic capacitances in real circuit implementation, a relatively larger 3σ matching accuracy is considered equal to 2%. Thus, the size of unity capacitor in 3-bit DAC of the proposed third-order incremental ADC is 19.8 μm × 19.8 μm and the corresponding 3σ matching accuracy is 0.1%.

B. Op-Amps Performance

In the scheme of Fig. 3, the design specifications of the first op-amp are more strict than what required from second and third op-amp. This is because any error caused by the first op-amp is accumulated quadratically, while the accumulation speed of errors introduced by the second and third op-amps is less.

Fig. 4 shows the simulated INL as a function of the first op-am DC gain. In this simulation, second and third op-amps are considered as ideal. As seen in Fig. 4, to keep the INL within 0.5 LSB, the minimum required gain for the first op-amp is 90 dB. A similar study for second and third op-amps has been performed as well. As shown in Fig. 5, the INL is well limited within ±0.5 LSB when the DC gains for the first, second and third op-amp are 95 dB, 90 dB, and 70 dB, respectively. The input is a constant signal ranging from $-V_{ref}$ to $+V_{ref}$. However, in the real circuit implementation, when the dynamic error caused by the op-amps finite bandwidth and slew rate are considered, some margin with respect to the previously mentioned values has to be taken.

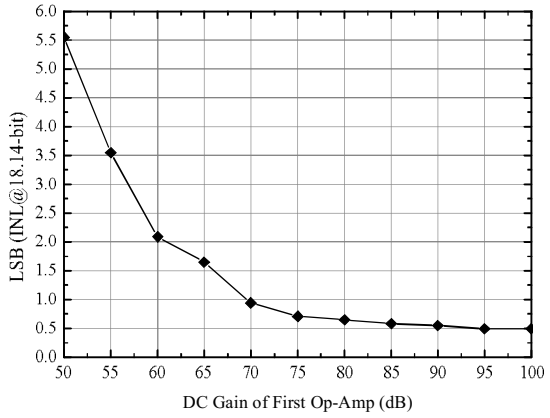

Fig. 4. INL as a function of the DC gain of the first op-amp.

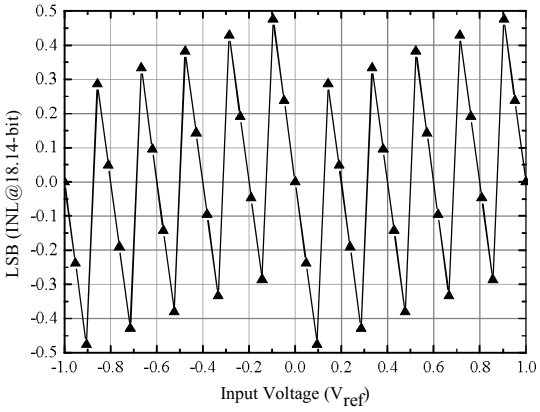

Fig. 5. INL of third-order incremental ADC with 95 dB, 90 dB and 70 dB gain for the three op-amps.

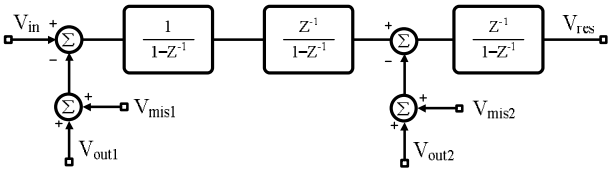

Fig. 6. Equivalent model of the proposed third-order incremental architecture.

Besides the DC gain, other important design parameters are op-amps bandwidth, slew rate and offset. Since incremental ADCs are always used for converting signal with low frequency, the sampling frequency of analog circuit normally is several MHz at most [2][4]. Hence, specifications on bandwidth and slew rate of op-amps generally are not difficult to achieve.

The offset of incremental ADCs should be carefully cancelled. For the third-order incremental architecture proposed in Fig. 3, the single-step chopping technique, [4], and fractal sequencing method, [7], can be well suited.

C. Mismatch of Multi-Level DACs and Compensation Methods

To study the effect of mismatch of multi-level DACs in the proposed third-order architecture, consider the equivalent model of Fig. 6. V_{out1} and V_{out2} are analog voltages corresponding to D_{out1} and D_{out2}. The error caused by mismatch among unity elements in DAC1, V_{mis1}, can be expressed as

$$V_{mis1} = \frac{V_{ref}}{8} \sum_{i=1}^{D_{out1}} W_{i,3ord} \times \epsilon_{i,dac1} \tag{9}$$

where $\epsilon_{i,dac1}$ is the error of the i-th unity element and

$$W_{i,3ord} = \frac{(N-i-1)(N-i-2)}{2!} \tag{10}$$

The error caused by mismatch of DAC2 is

$$V_{mis2} = \frac{V_{ref}}{8} \sum_{i=1}^{D_{out2}} W_{i,1ord} \times \epsilon_{i,dac2};\ W_{i,1ord} = 1 \qquad (11)$$

Since the weight of the errors, $W_{i,3ord}$, for DAC1 case is dependent on the clock period in which the error is injected, a third-order Smart-DEM algorithm, [8], can be used to compensate for that errors. For DAC2 the situation is different. As it can be seen in (11), $W_{i,1ord}$ is a constant number and thus also a conventional DWA DEM algorithm can be adopted.

IV. Simulation Results

To demonstrate the adopted mismatch compensation strategy effectiveness for this third-order incremental architecture, two groups of behavioral level simulations have been performed. Fig. 7 shows the performance comparison of the third-order scheme in three different cases. The mismatch for unity elements of both DAC1 and DAC2 obeys normal distribution with zero mean value with $3\sigma = 0.1\%$. The input is a constant voltage ranging from $-V_{ref}$ to $+V_{ref}$. The maximum INL without compensation is about 49.9 LSB. When using the DWA method for both DACs, the error is not linear with a maximum of 1.8 LSB. The use of Smart-DEM algorithm for DAC1 and DWA DEM for DAC2 is able to keep the error within 0.5 LSB for entire range.

For the second group of simulations, the mismatch for DACs unity elements is larger: it obeys normal distribution with zero mean value and $3\sigma = 0.5\%$. The maximum INL without compensation is 205.7 LSB. With DWA method for DAC1 and DAC2, the maximum error is 6.1 LSB. The Smart-DEM is able to keep the error within 0.5 LSB for entire range even for such a large mismatch.

V. Conclusion

Multi-bit quantization in incremental modulators is possible only if the unity elements mismatch is carefully compensated for. The conventional DEM methods used for ΣΔ modulators are not suitable for incremental schemes. On the contrary, the Smart-DEM algorithm is able to compensate for the mismatch of both second-order and third-order schemes. In this paper, a 2+1 incremental architecture is proposed, which uses third-order Smart-DEM algorithm for the first DAC, while DWA method is adopted for the error correction of second DAC. Extensive behavioral simulations verify the effectiveness of the approach. This 2+1scheme is able to achieve 18-bit resolution with only 61 clock periods.

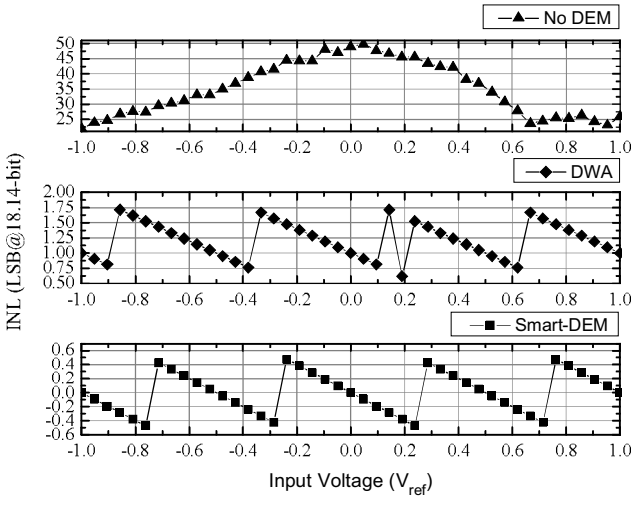

Fig. 7. Performance comparison for third-order incremental: without DEM (top), with DWA for DAC1 and DAC2 (middle) and with Smart-DEM for DAC1 and DWA for DAC2 (bottom). The mismatch of unity elements of both DAC1 and DAC2 obeys normal distribution with zero mean and $3\sigma = 0.1\%$.

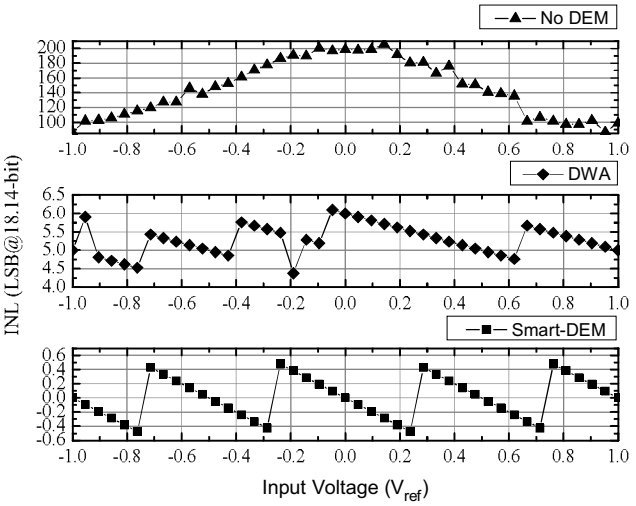

Fig. 8. Performance comparison for third-order incremental: without DEM (top), with DWA for DAC1 and DAC2 (middle) and with Smart-DEM for DAC1 and DWA for DAC2 (bottom). The mismatch of unity elements of both DAC1 and DAC2 obeys normal distribution with zero mean and $3\sigma = 0.5\%$.

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