Sampled-Data Operational-Amplifier with Ultra-Low Supply Voltage and Sub μW Power Consumption

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***Abstract*—This paper proposes the use of sampled-data operation in op-amps. The technique favors very low supply voltage and micro-power. After discussing the method at a general level, a possible sampled-data scheme is analyzed. Simulations with a low threshold technology show that a 0.5-V supply is possible. A version of the circuit, which has been integrated by using a standard 0.18-μm CMOS technology (with high thresholds), is able to operate at 0.65-V supply voltage. Simulation results show 42.5 dB of DC gain and 2.5-kHz bandwidth with 0.5-pF load capacitor. The power consumption is 63 nW. A pseudo-differential scheme doubles the consumed power and increases the DC gain by 6 dB.**

I. Introduction

Circuits for nomadic electronics require ultra-low power and very-low supply voltage. Optimally, it would be necessary using a supply voltage of 0.5-0.6 V because this is the voltage range at the output of a single solar cell [1]. Digital circuits can work with such low voltages, since their required supply voltage is just a bit more than the threshold of an n-channel or a p-channel transistor. On the contrary, conventional analog amplifiers need higher supply voltage due to the required overheads at the output stage and the necessary output swing.

The band of signals handled in many sensor applications is narrow and the speed is not important. Instead, low-power is a relevant design feature. Indeed, the power harvested indoor by a solar cell battery is around tens of μW/cm^2 [2]. Therefore, the power consumed by a single analog cell can be in the hundreds of nW range.

Low supply voltage implies low signal-to-noise ratio (SNR): the voltage swing of the signal is low, but the noise remains the same. This is a problematic issue. However, at the same time, it allows moderating the analog performance requirements. For instance, a large DC gain in op-amps is not as important as before, since the errors due to the value and non-linearity become negligible for the expected SNR.

The presented sampled-data op-amp is a suitable answer to the above needs. The supply voltage of the proposed circuit, realized with a technology with relatively low thresholds, is as low as 0.5 V. The simulated DC gain is 42.5 dB while the power consumption is 63 nW. The gain becomes more than 48 dB with a pseudo-differential scheme which consumes 126 nW.

II. Sampled-Data Operational Amplifier

When the signal band is small, it can be convenient to use sampled-data operation. There are many examples of sampled-data systems for realizing filtering functions or for data conversion [3]–[5]. This paper proposes using the sampled data technique even at the op-amp level. It results that the output voltage of the op-amp changes in a discrete manner under the control of a clock with a frequency higher than the frequency of the system where that op-amp is used. Fig. 1 shows the conceptual scheme of the sampled-data op-amp. A toggle capacitor C_0 is charged at A_0V_d during Φ_1. During Φ_2, it shares its charge with the load capacitance C_L and the feedback network. In the inverting integrator configuration shown in Fig. 1, each injection of charge by the switched capacitor C_{in} gives rise to a pseudo-exponential transient with time-constant $C_T/(TC_0)$ (C_T is the total capacitive load and T is the clock period) or a ramp when it operates in the pseudo slew-rate region. An example of the output waveform for a negative input signal is also given in Fig. 1.

The power consumed by the sampled-data op-amp is the one of the pre-amplifier plus the dynamic power of the toggle capacitor, $(V_{DD}/2)^2C_0/T$. The latter, for V_{DD} = 0.5 V and C_0 = 0.2 pF, is less than 1 nW with $f_s = 1/T$ = 50 kHz. Therefore, the power required by the pre-amplifier dominates

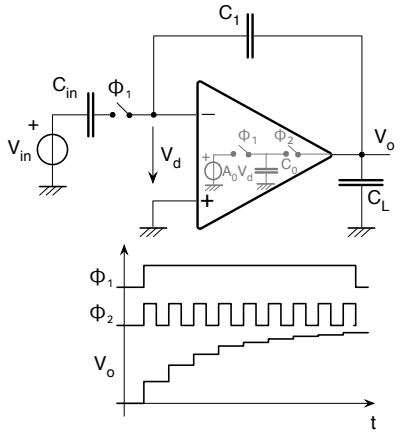

Fig. 1. Conceptual scheme of the sampled-data op-amp used in an inverting integrator configuration.

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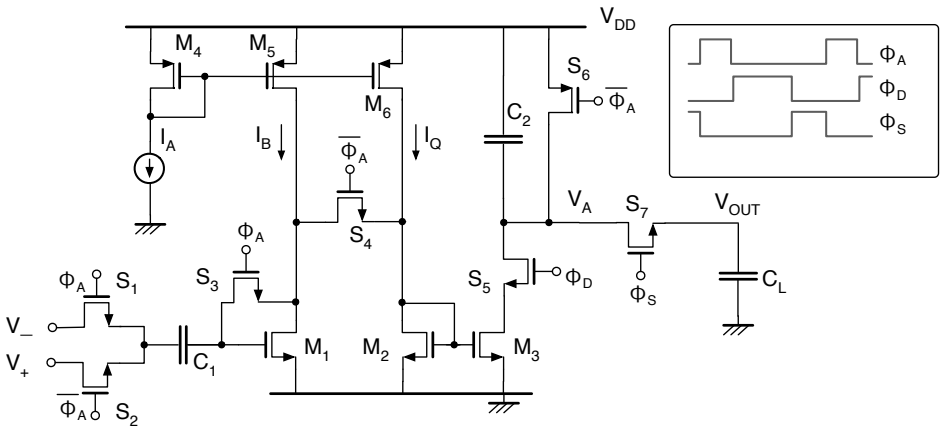

Fig. 2. Schematic of the proposed sampled-data amplifier.

the power consumption of the part.

A. Sampled-Data Amplifier

Fig. 2 shows the proposed sampled-data amplifier. It operates under the control of three phases. The first phase, Φ_A, connects the input transistor M_1 in the diode configuration to charge the auto-zero capacitor C_1 to V_- minus the V_{GS} of the input transistor M_1. The second phase, Φ_D, is the amplification phase. The signal current, i_d, flows through the switch S_4 into M_2 and mirrored to charge the capacitor C_2 for the fixed time set by Φ_D. The bias current I_Q determines the quiescent discharge voltage. The switched capacitor output structure, controlled by Φ_S, provides the output. The differential inputs and the transconductance of the input transistor M_1, which operates in sub-threshold region, give rise to the charging signal current:

$$i_d = g_{m_1}(V_+ - V_-) = \frac{I_B}{nV_T}(V_+ - V_-) \tag{1}$$

where I_B is the current in M_1, n the sub-threshold region slope and V_T the thermal voltage.

It is easy to verify that the DC gain of the sampled-data amplifier of Fig. 2 is

$$A_0 = \frac{i_d T_D}{C_2} = \frac{I_B}{nV_T}\frac{T_D}{C_2} \tag{2}$$

which depends on three parameters: the bias current in M_1, the charge time and the value of C_2. For I_B = 100 nA, T_D = 10 µs and C_2 = 0.2 pF, the calculated gain is around 40 dB.

The quiescent output voltage, V_Q, depends on the quiescent current I_Q, the charge time and the value of C_2. If the signal current is zero, V_Q is

$$V_Q = V_{DD} - \frac{I_Q T_D}{C_2} \tag{3}$$

that, for V_{DD} = 0.5 V and the above used parameters, leads to I_Q = 5 nA to obtain $V_Q = V_{DD}/2$.

Observe that the circuit of Fig. 2 does not exactly correspond to the equivalent circuit given in Fig. 1. The voltage across the capacitor C_2 is not generated by a voltage source, but results from the current $I_Q + i_d$ charging C_2 during the period T_D. However, that is equivalent to the action of a voltage generator.

B. Circuit Implementation

The circuit of Fig. 2 has been designed and simulated at the transistor level using a low threshold 0.18-µm CMOS technology ($V_{th,n}$ = 0.15 V, $V_{th,p}$ = −0.18 V). The current in the bias generator M_4 is 10 nA with W/L = 4. The aspect ratios of transistors M_5 and M_6 are 40 and 2, respectively, to have nominal currents I_B = 100 nA and I_Q = 5 nA. The capacitor C_1 used for storing the input offset during the auto-zero period is 2 pF. The clock frequency is 50 kHz (T = 20 µs) with auto-zero phase, Φ_A, 25% and amplification phase, Φ_D, 50% of the clock period.

The switches are realized by single NMOS or PMOS transistors. In order to ensure a low on resistance, the amplitude of the phase controlling the NMOS switches is 1 V which is requiring a simple clock boost on chip. Therefore, switches S_1 and S_2 operate properly while the common mode input voltage is 0.25 V. Any other input common mode value can be admitted, provided that the two switches are working as required. Table I gives the transistors sizes of this 0.18-µm CMOS design.

The accuracy of the DC gain depends on the accuracy of the Φ_D period. A possible jitter in T_D, δT_D, changes the gain by δA_0. The sensitivity is

$$\frac{\delta A_0}{A_0} = \frac{\delta T_D}{T_D} \tag{4}$$

which is very low for the designed value of T_D (=10 µs) and the jitter of a normal phase generator.

It is possible to increase the DC gain by changing the design parameters of equation (2) or by increasing the mirror factor between M_2 and M_3. Since even the bias current I_Q augments, it is necessary to compensate for its effect on the output stage with an additional branch. The transistor M_7 supplies a current $(N-1)I_Q$ as shown in Fig. 3 to set the quiescent current used to charge C_2 to the expected value I_Q.

TABLE I. TRANSISTOR SIZES OF SAMPLED-DATA AMPLIFIER

Transistor	W/L
M_1	100 µm / 1 µm
M_2, M_3	5 µm / 1 µm
M_4	20 µm / 5 µm
M_5	200 µm / 5 µm
M_6	10 µm / 5 µm
S_1, S_2, S_7	0.22 µm / 0.18 µm
S_4, S_5, S_6	5 µm / 0.18 µm

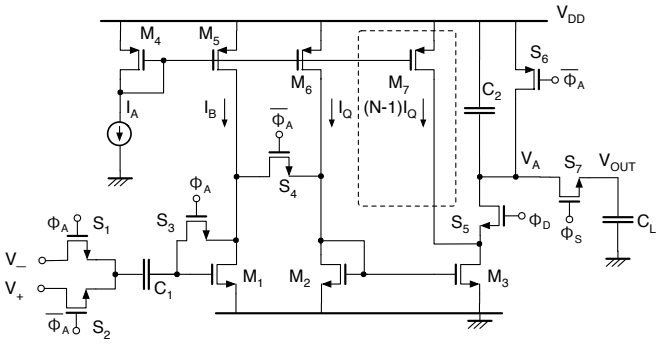

Fig. 3. Schematic of the sampled-data amplifier with the modification to increase the gain.

III. SIMULATION RESULTS

The transient level simulations confirm the expected circuit operation. The supply voltage is 0.5 V and, with zero differential input signal, the output voltage becomes 254 mV. The switching off of S_6 and the switching on of S_7 cause a limited clock feedthrough, as shown in Fig. 4. This corresponds to a small input referred offset. Fig. 4 shows the discharge transients of C_2 for various differential inputs. When the differential input voltage is more than ±3.5 mV, the output almost saturates to the supply levels. The behavior is slightly asymmetrical.

When the switches do not work properly, for instance when the amplitude of the clock phase is reduced to 0.5 V, the circuit performance worsens significantly. Having a good overdrive for the transistors that realize the switches is essential. For this reason, the phases must have a relatively large amplitude.

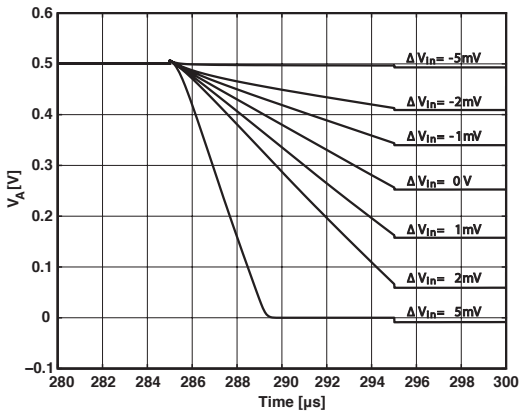

Fig. 4. Discharge transients for various differential inputs.

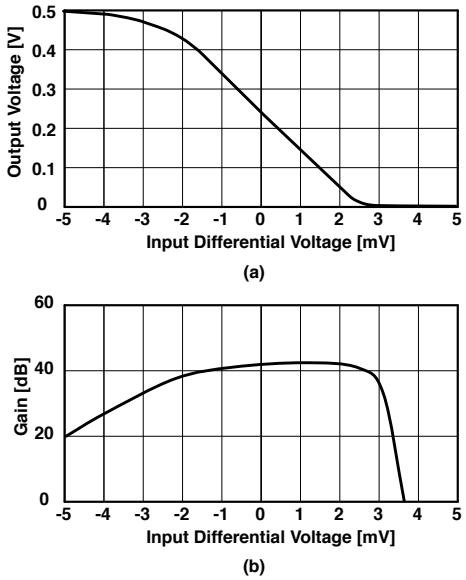

Fig. 5. (a) Simulated amplifier input-output characteristic. (b) Differential gain as a function of the input differential voltage.

A simple clock boost [6] realized with a 0.2-pF boosting capacitor resolves the problem. Its dynamic power consumption is less than 2 nW. The total consumed power of the circuit with V_{DD} = 0.5 V is 63 nW.

The input-output characteristic is given in Fig. 5 (a). With a negative signal current, the charge drained from C_2 diminishes and the output voltage ($V_A = V_{DD} - V_{C2}$) increases. A positive signal current speeds up charging and the output voltage becomes smaller. The asymmetry of the response is evident from Fig. 5 (b), which shows the small signal gain. The maximum gain is more than 42 dB. However, there is a tilt in the range around V_d = 0. The use of the pseudo-differential version shown in Fig. 6 (a) leads to the symmetrical gain curve of Fig. 6 (b). The peak gain is 48.2 dB at the cost of doubling

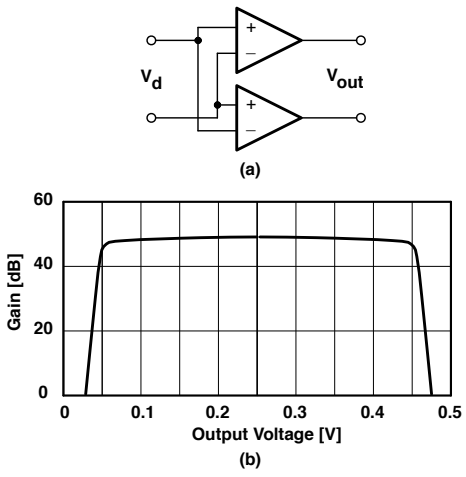

Fig. 6. (a) Pseudo-differential configuration. (b) Small signal differential gain as a function of the output voltage.

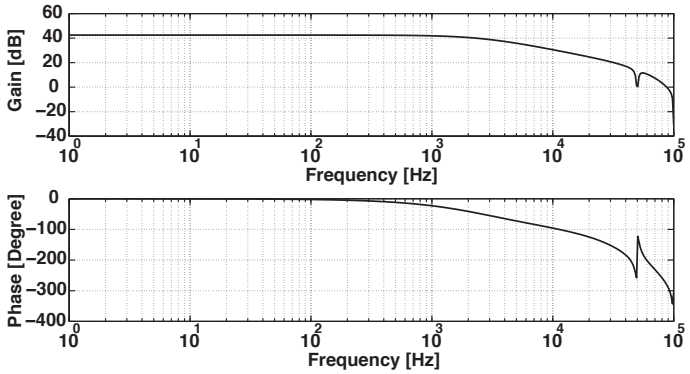

Fig. 7. Simulated frequency response of the sampled-data amplifier.

the power consumption (126 nW).

Periodic steady state and periodic AC analysis estimate the frequency response of the sampled-data amplifier. The gain and the phase plots of the single ended version are shown in Fig. 7. The DC gain is 42.45 dB and the bandwidth is 2.5 kHz. Since the clock frequency is 50 kHz, there are zeros at that frequency and its multiples.

The power supply rejection ratio performance is poor, as shown in Fig. 8, since any variation of the supply voltage becomes an equal variation at output. The obvious recommendation is using the pseudo-differential configuration that increases the DC gain by 6 dB, but, more importantly, well rejects spurs coming from the power supply.

Fig. 9 shows the transient simulations of the proposed sampled-data amplifier when closed in the inverting integrator configuration of Fig. 1. The simulation uses $C_{in} = C_1 = 0.5$ pF and $C_L = 1$ pF. With an input signal of -100 mV, the integrator output voltage (top waveform of Fig. 9) settles pseudo-exponentially to 350 mV in 15 clock cycles. Fig. 9 also gives the virtual ground and the V_A (see Fig. 2) nodes transient responses (middle and bottom waveforms). The virtual ground node reaches the input common mode level of 200 mV, while the voltage V_A determines the integrator output voltage level. From the figure, it can be noted how the amplifier operates in the slewing mode for the first 7-8 clock cycles, before settling exponentially.

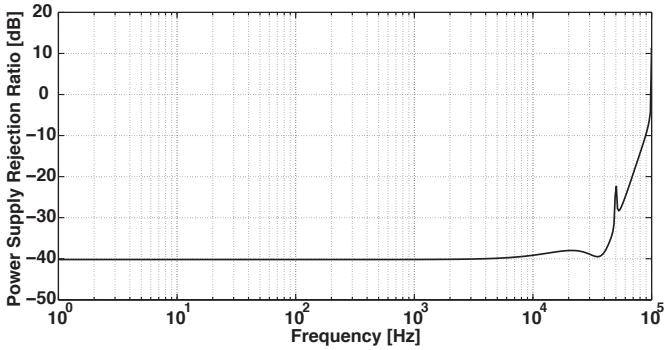

Fig. 8. Simulated power supply rejection ratio of the sampled-data amplifier.

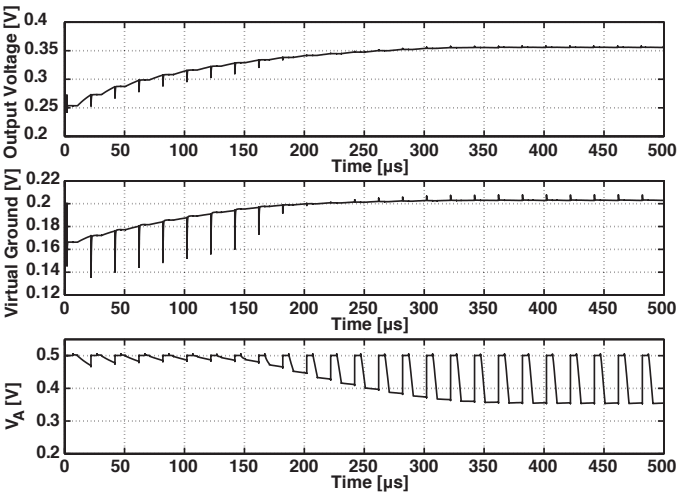

Fig. 9. Simulated transient response of the proposed sampled-data amplifier closed in the inverting integrator configuration.

IV. Conclusion

The sampled data method applied to the op-amp leads to ultra-low voltage operation and extremely low power. Since the method affects the speed, the proposed approach is a valid solution for processing signals with few tens of Hz of bandwidth. In this paper, a sampled-data amplifier design and simulation results are presented by using a 0.18-µm CMOS technology with low threshold transistors. The designed amplifier achieves 42.45 dB of DC gain and 2.5-kHz bandwidth with 0.5-pF load capacitor while using 0.5-V supply voltage. The power consumption of the circuit is 63 nW and the PSRR is around -40 dB. The DC gain of the sampled-data amplifier can be doubled by utilizing a pseudo-differential architecture which is also recommended to well reject the spurs coming from supply voltage, at the cost of doubling the consumed power and area.

Acknowledgment

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References

[1] N. Bourgoine, "Harvest Energy from a single Photovoltaic Cell", *Journal of Analog Innovation*, vol. 21, no. 1, April 2011.

[2] M. Raju and M. Grazier, "ULP meets energy harvesting: a game-changing combination for design engineers", *Texas Instruments, White Paper, Energy Harvesting*, April 2010.

[3] K.R. Laker, W. M. C. Sansen, "Design Of Analog Integrated Circuits And Systems", McGraw-Hill, 1994.

[4] R. Schreier and G.C. Temes, "Understanding Delta-Sigma Data Converters", New York: Wiley-IEEE, 2005.

[5] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Markus, J. Silva, and G.C. Temes, "A low-power 22-bit incremental ADC", *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562-1571, May 2005.

[6] M. Keskin, "A low-voltage CMOS switch with a novel clock boosting scheme", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 4, pp. 185-188, April 2005.