A Split Transconductor High-Speed SAR ADC

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***Abstract*—A feasibility study of an 8-bit fast converter is presented. The advantages and limits of conventional SAR architectures are discussed and, on the basis of that, a possible optimal architecture is proposed. It uses a 4+4-bit scheme with combination of the DAC outputs in the current domain at the input of the latch. The circuit has been implemented with a 28 nm FDSOI CMOS technology. Post layout simulation results show 8-bit of resolution at 1.2 GS/s.**

I. Introduction

Data converters with low-medium resolution operating at sampling-rate in the multi GS/s frequently use time interleaved architectures of SAR converters, [1] [2]. They exploit the advantage of low power and relatively low consumed area, as required for using a large number of interleaved channels. The DAC used in the SAR feedback loop is typically capacitive-type with a binary array of unity elements. The technology, the kT/C limit, and the matching between capacitors determine the value of the unity elements. For a reference voltage of 1 V and 8-bit resolution, the kT/C condition puts the limit to very small values: the overall capacitive array must be less than 3.2 fF. Therefore, possible limits come from technology and capacitive matching. We considered two technologies: 65 nm and 28 nm CMOS. The 65 nm process provides unity MOM capacitors whose minimum value is 8 fF. The 28 nm technology allows unity MOM capacitors of 2 fF when using two metal layers and 4.4 fF with all the metal layers. This would give rise to plain 8-bit binary arrays of 2 pF, 1.1 pF, and 0.5 pF total capacitance, respectively. With a split 4+4-bit architecture, capacitances diminish by a factor 32.

The specific capacitances and the matching (at 3σ) between unity capacitors determine the minimum size of the unity elements. Since the maximum error occurs at half-scale, we consider the mismatch between two halves of the array. Table 1 summarizes the results. It shows that a plain 8-bit array with minimum unity capacitor ensures resolution above 9 bit. However, the architecture with minimum capacitive array and able to ensure 8 bit of resolution is the 28 nm with all the metal layers used to realize the MOM unity capacitance.

Simulations with the 65 nm CMOS and the 28 nm CMOS technology show that minimum width transistors with W/L = 4 and V_{GS} = 1 V (we assume to use clock boost, [3])) achieve on-resistances equal to 730 Ω and 570 Ω, respectively. Since achieving 8-bit accuracy requires at least 6 time constants, an adequate sampling of the input signal with two series switches within 180 ps needs an $R_{on}C_{array}$ lower than 34 ns. This leads to the aspect ratio of the switches used for sampling indicated in the Table. The value for the 28 nm technology and unity capacitors of 4.4 fF is large but affordable.

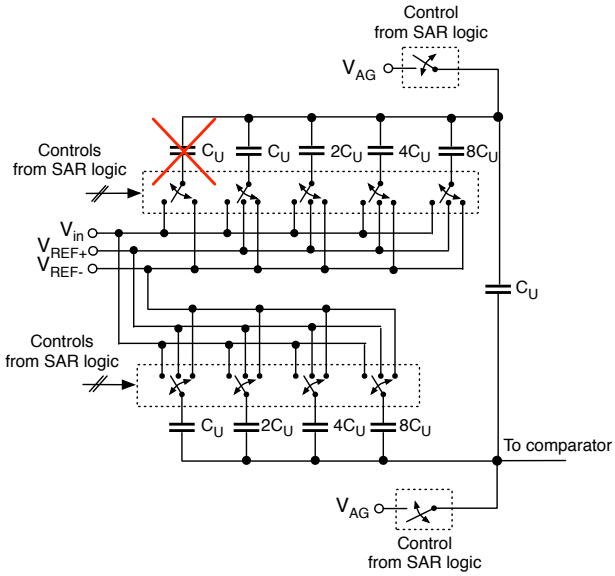

Fig. 1. 4+4 split SAR topology.

The result of this introductory study indicates that, for the design of an 8-bit SAR with very high sampling rate, the optimal solution is a split architecture with 4+4-bit realized with a 28 nm CMOS process. This paper describes the possible circuit implementation. It uses two 4-bit SARs but avoids the limits of the conventional architecture that employs an attenuating capacitor between the two SAR arrays.

II. System Architecture

A. Standard Topology and Limitations

Fig. 1 shows the architecture of a conventional 4+4 split SAR. The value of the attenuation capacitor is $8C_U/7$. Having a non-unity element is problematic; however, the limit can be transformed into a gain error of 1 LSB by removing a unity capacitor, as shown in the figure, [4]. Another limit of the split SAR scheme comes from the parasitic capacitances. When using very small unity elements, the capacitance of metal routing becomes significant and influences the attenuation factor, [5] [6] [7]. This requires digital calibration, [8], that, for a 28 nm technology and C_U = 4.4 fF, becomes necessary even for 8-bit accuracy.

The comparator can be a simple regenerative latch or a transconductance pre-amplifier followed by a regenerative latch. Since for 8-bit accuracy and 1 V reference the LSB is

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TABLE I. PLAIN 8-BIT AND 4+4-BIT SAR ADCS: TECHNOLOGY AND CAPACITIVE MATCHING

Architecture and Technology [nm]	8-b 65	8-b 28 (All layers)	8-b 28 (2 layers)	4+4-b 65	4+4-b 28 (All layers)	4+4-b 28 (2 layers)
Minimum MOM capacitor [fF]	8	4.4	2	8	4.4	2
Total capacitor array size [fF]	2048	1126.4	512	256	140.8	64
Specific capacitance [fF/μm^2]	1.65	1.1	0.5	1.65	1.1	0.5
Total array area [μm^2]	1241.2	1024	1024	155.15	128	128
3σ matching accuracy [%/μm]	0.08	0.045	0.065	0.08	0.045	0.065
Error [‰]	1.6	0.99	1.57	4.54	2.81	4.45
Resolution number of bit	9.28	9.97	9.31	7.78	8.47	7.81
Switches aspect ratio	394	169	77	49	21	10

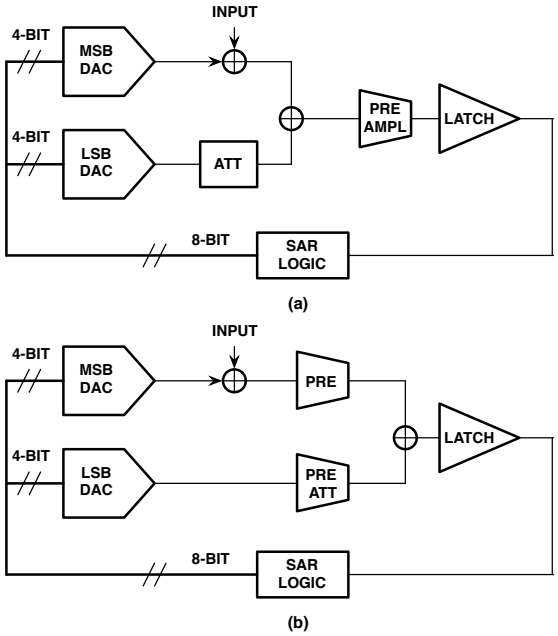

Fig. 2. Split SAR equivalent topologies.

4 m V, the use of a pre-amplifier is recommended, because a larger signal at the latch input better faces metastability. For both cases, the kick-back of the comparator generates transients on the top plates of the capacitive arrays, especially on the one used for the LSBs. The attenuating capacitor protects that array only partially.

B. Proposed Topology

The split SAR architecture of Fig. 1 corresponds to the equivalent schematic of Fig. 2(a). The input of the transconductor used before the latch is the input signal minus the two output DACs, one of this attenuated by a 2^4 factor. Fig. 2(b) shows the proposed alternative topology. The pre-amplification function is performed by two transconductors and the attenuation factor is incorporated into the lower transconductor. Possibly, the attenuation factor can be shared between the transconductor and the LSB DAC. The advantage of the new topology is a better insulation of the DAC used for the MSBs from the one used for the LSBs. Moreover, for determining the LSB with the convention split SAR architecture, the LSB DAC must drive the array of the MSB DAC. As verified by extensive computer simulations at the transistor level, the speed of the new architecture is higher than the conventional one.

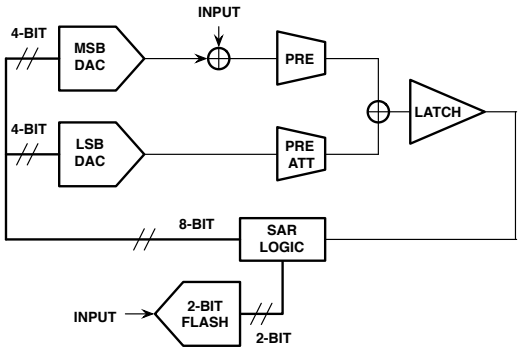

Fig. 3. Modified split SAR equivalent topologies.

The key request for the proposed topology is to ensure a linearity of the transconductor better than 0.25% over the full input signal swing. This is obviously very difficult, especially before generating the first bits of the digital output. In order to limit the request, the architecture is modified as shown in Fig. 3. There is a second sampling of the input used in a 2-bit flash converter. The extra cost is limited because the operation requires three comparisons instead of two. Having determined two bits, the MSB channel generates at the input of the transconductor a signal with ±125 mV (the full scale is 1 V). Therefore, the linearity request is for a relatively low voltage range. The use of the flash also augments the speed because the architecture determines two bits with a single time slot. Even for the SAR, it is possible to determine 2-bit per cycle. This requires using three comparators with suitable

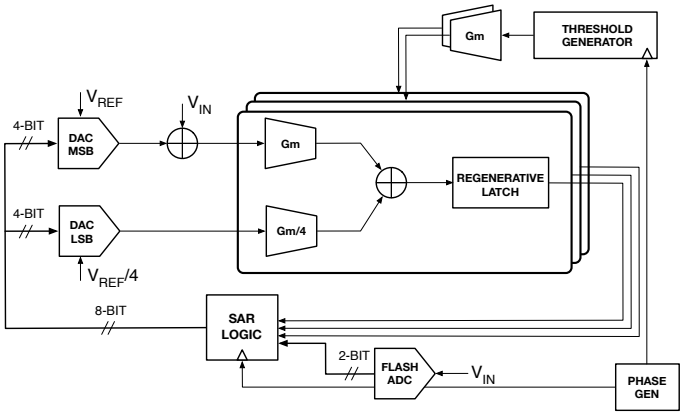

Fig. 4. SAR ADC architecture.

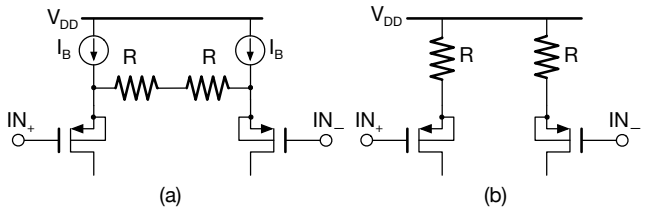

Fig. 5. Schematic of fast transconductors.

shifts of the thresholds. Fig. 4 shows the obtained architecture. It uses three latches and three replicas of the pre-amplifier transconductors. For two of them there are extra input currents shifting the thresholds under the control of the timing logic. The voltages used to shift the threshold ask for calibration in the foreground.

C. High-Speed Transconductors

The transconductors of the architecture must be at the same time linear and fast. This study foresees working periods of 91 ns derived by a main clock of 5.5 GHz. A period is for the regenerative latch, another for the SAR logic and the transconductor response. The simple scheme of Fig. 5(a) ensures a very fast response with bias currents in the few hundreds of μA range. However, the linearity is limited by the non-linear dependance with current of the overdrive voltage of the p-channel transistors and the output resistance of the current sources. Across them, it is necessary to ensure a relatively large voltage to be far enough from the triode region. Fig. 5(b) shows an alternative pseudo-differential solution. The quiescent current depends on the resistors value and the common-mode voltage at the differential inputs. This is the setting voltage on the top of the capacitive arrays established during the sampling phase. In first approximation, the large signal current is

$$\Delta I = \frac{\Delta V}{R + \frac{1}{G_m}} \tag{1}$$

In order to ensure linearity, the resistor value must dominate the denominator. With R = 500 Ω, the linearity allows 8 bit of resolution.

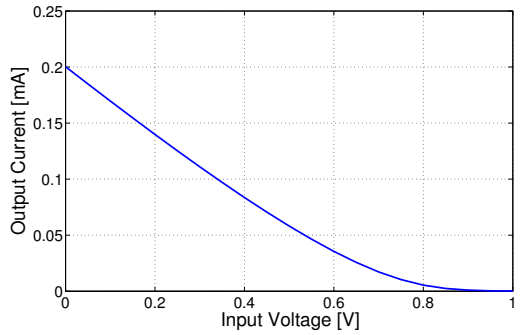

Fig. 6. Current-voltage response of the transconductor of Fig. 5.

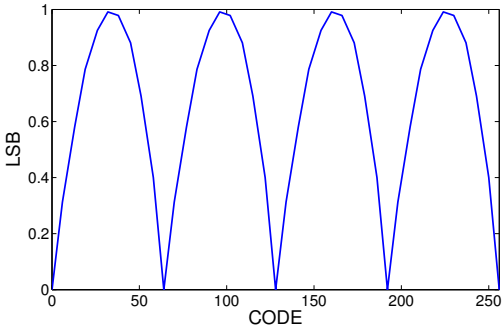

Fig. 7. INL of the transconductor of Fig. 5.

Fig. 6 shows the simulated current-voltage response of the transconductor. The linearity of the response is good with input around 300 mV. This is the value of V_{AG} used in the design. The range of operation is ±125 mV around the quiescent value. Fig. 7 plots the expected INL caused by the transconductor. Its limits are within ±0.5 LSB.

D. Comparator Design

Fig. 8 shows the circuit diagram of the full comparator. It includes the transconductors and the latch. The regenerative latch uses a double loop to speed up the operation. However, the nMOS loop is stronger, while the pMOS loop, designed with minimum size transistors, enhances the speed with minimum capacitive load on output nodes. M12-M13 open during recharging phase; small sizes of M10-M11 make minimum the capacitive load.

The power consumption of the comparator depends on the dynamic power of the latch and on the static power of transconductors. For a given technology, there is an optimum design that maximizes the speed of the latch. The optimal design requires a given input quiescent current and, consequently, a given consumed power. Fig. 9 shows the relationship between the total consumed power and the comparator decision time. With low power (100 μW), the latch responds in 66.5 ps. In order to speed up by 5% the decision time, it is required to triplicate the consumed power. A suitable safety margin suggests to operate with 200 μW consumption. The diagram of Fig. 9 also indicates that increasing power consumption does not increase the speed. Therefore, architectures with 2b/cycle instead of 1b/cycle are the only viable solution for speeding up the system.

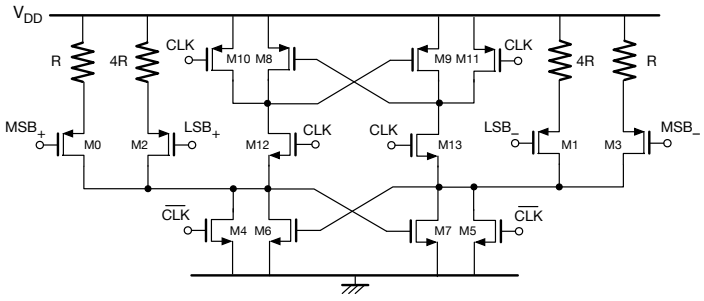

Fig. 8. Schematic diagram of the voltage comparator.

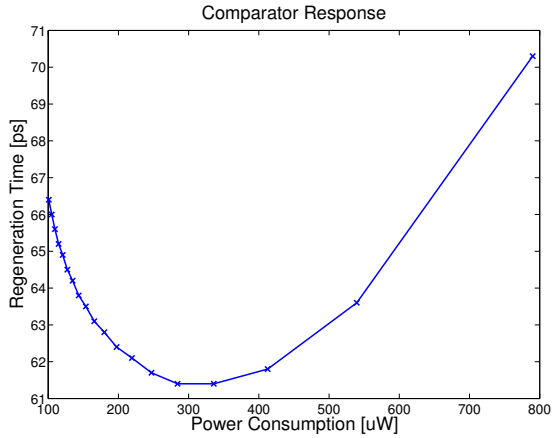

Fig. 9. Comparator decision time as a function of the comparator power consumption.

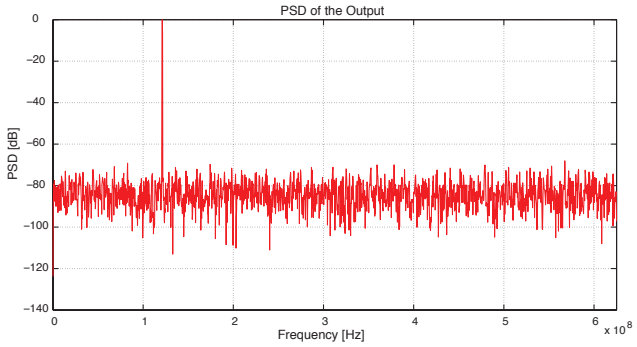

Fig. 10. Simulated output spectrum at 1.1 GS/s with a 121-MHz input signal.

III. Simulation Results

The proposed scheme has been post layout simulated (in nominal conditions) with a 28-nm FDSOI CMOS technology. The nominal supply voltage is 1 V and the clock frequency is 5.5 GHz (1.2 GS/s).

Fig. 10 shows the simulated output spectrum with a full scale sinusoidal input signal at 121 MHz. The fft has 4096 points. The achieved signal-to-noise (SNR) ratio is 49.4 dB, equivalent to 7.9 bit of resolution.

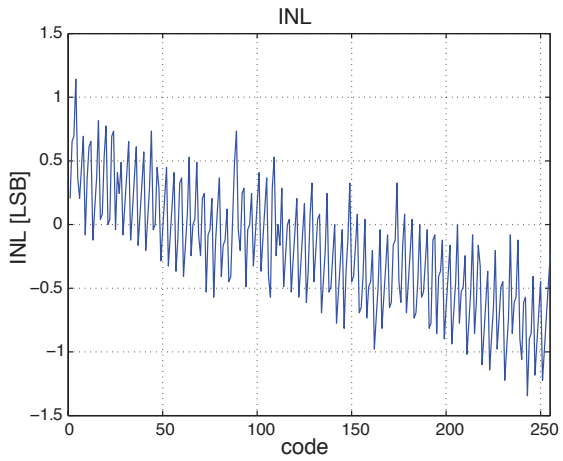

Fig. 11. Simulated INL.

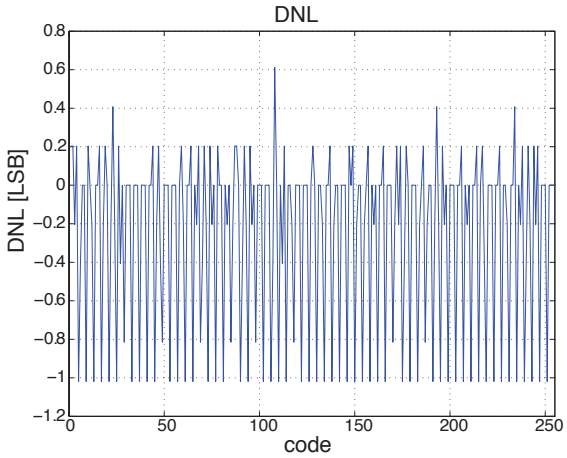

Fig. 12. Simulated DNL.

Fig. 11 and Fig. 12 show the simulated integral nonlinearity (INL) and differential nonlinearity (DNL), respectively. The peak INL and DNL are 1.14/−1.35 LSB and 0.61/−1.02 LSB, respectively.

The results of this feasibility study verify the possibility to achieve 8 bit of resolution and 1.2 GS/s conversion rate with a 28-nm CMOS technology. This almost corresponds to the state of the art.

References

[1] L. Kull, T. Toifl, M. Schmatz, P.A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T.M. Andersen, Y. Leblebici, "A 90GS/s 8b 667mW 64x Interleaved SAR ADC in 32nm Digital SOI CMOS", *IEEE International Solid State Circuits Conference (ISSCC) Dig. Tech. Papers*, pp. 378-379, Feb. 2014.

[2] S. Le Tual, P.N. Singh, C. Curis, and P. Dautriche, "A 20GHz-BW 6b 10GS/S 32mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology", *IEEE International Solid State Circuits Conference (ISSCC) Dig. Tech. Papers*, pp. 382-383, Feb. 2014.

[3] A.M. Abo and P.R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", *IEEE Journal of Solid State Circuits*, Vol. 34, No. 5, pp. 599-606, May 1999.

[4] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "An Ultra-Low Power Successive Approximation A/D Converter with Time-Domain Comparator", *Analog Integrated Circuits and Signal Processing*, vol. 64, pp. 183-190, Aug. 2010.

[5] Y. Zhu, C.-H. Chan, U.-F. Chio, S.-W. Sin, S.-P. U, R.P. Martins, and F. Maloberti, "Split-SAR ADCs: Improved Linearity with Power and Speed Optimization", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 22, No. 2, pp. 372-383, Feb. 2014.

[6] W. Guo and S. Mirabbasi, "A Low-Power 10-bit 50-MS/s SAR ADC Using a Parasitic-Compensated Split-Capacitor DAC", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1275-1278, May 2012.

[7] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure", *IEEE Journal of Solid State Circuits*, Vol. 45, No. 4, pp. 731-740, April 2010.

[8] M. Yoshiota, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10-bit 50-MS/s 820-μW SAR ADC with On-Chip Digital Calibration", *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 4, No. 6, pp. 410-416, Dec. 2010.