Design of a Low Power Time to Digital Converter for Flow Metering Applications

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***Abstract*—This paper presents the design of an hybrid course-fine time to digital converter for low power applications. The core of the circuit consists of two current-mode SAR analog to digital converters working in a time-interleaved fashion. The TDC has been fully simulated at the transistor level with a 0.13-μm CMOS technology. The paper discusses the design details and the digital calibration techniques required to achieve a single-shot resolution of about 27 ps while keeping the power consumption below 600 μW.**

I. Introduction

Ultrasonic techniques are widely used for flow metering applications in both medical and industrial fields, [1] [2]. Ultrasonic flow meters present evident advantages with respect to other known methods (such as turbine, Venturi and others) to measure the volumetric flow rate of a fluid: measurement does not require any moving parts which implies low maintenance cost, is non-intrusive thus resulting in low pressure drop, and the equipment can be eventually portable. Among the different ultrasonic methods (Doppler, cross-correlation, sing-around) for flow metering, the transit-time based flow meter is widely adopted.

The ultrasound transit-time flow meter is based on a well established principle. Two ultrasonic transducers are placed in different positions face to face on a pipe so that the sound pulses emitted from one transducer can be collected by the other, as shown in Fig. 1. Due to the fluid flowing, the transit-times of upstream, T_{up}, and downstream, T_{down}, pulses are different. Being known the geometry of the system and by measuring T_{up} and T_{down}, the expression of the fluid velocity can be estimated as:

$$v = \frac{L(T_{up} - T_{down})}{2T_{up}T_{down}cos(\alpha)} \quad (1)$$

where α is the angle indicated in the scheme of Fig. 1. It is, hence, evident that the main challenge in the design of transit-time based ultrasonic flow meters is the accurate measurements of the upstream and downstream times.

Time to digital converters (TDCs) provide the conversion of a time interval into a digital number, [3]. They are now being used in many applications such as laser range finders, space science instruments, measurement devices and, more recently, they are employed to measure phase in all-digital phase-locked loops. A TDC can be realized as a single counter by means of simple time comparators (D-type flip-flops) and other basic digital cells. With the same building blocks, Flash TDCs and Vernier oscillators have been designed, [4] [5].

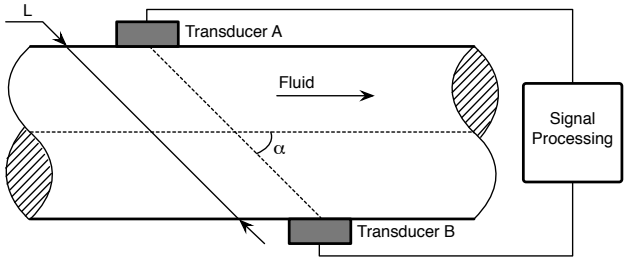

Fig. 1. Conceptual scheme of a transit-time ultrasonic flow meter.

Despite their simplicity, these schemes cannot resolve the time interval better than a single buffer delay. More complex schemes overcome the drawback at the expense of an increased area and power consumption. The gated-Vernier scheme described in [6] provides an equivalent resolution of 3.2 ps with a relatively large power consumption of 3.6 mW. Other TDCs architectures are inspired to analog-to-digital converters (ADCs) schemes. The coarse-fine TDC reported in [7] achieves 1.25-ps resolution while consuming 3 mW while a TDC based on the successive approximation interpolation method, [8], achieves a resolution of about 1.2 ps but the power consumption is as large as 33 mW.

The target application of this design is water flow metering based on the ultrasound transit-time (or time of flight) method. The application uses low power ultrasonic transducers and requires medium one-shot resolution (better than 30 ps) for a typical time of flight of about 50 μs with a power consumption lower than 500 μW. This paper presents the design of an hybrid time to digital converter with coarse conversion achieved with a digital counter and fine conversion obtained by two analog channels based on a SAR ADC scheme. The circuit, designed with a standard 0.13-μm CMOS technology, has been simulated at the transistor level and simulation results verify the target design specifications.

II. System Architecture

The block diagram of the flow meter electronic system is shown in Fig. 2: it is composed by an analog front-end (AFE),

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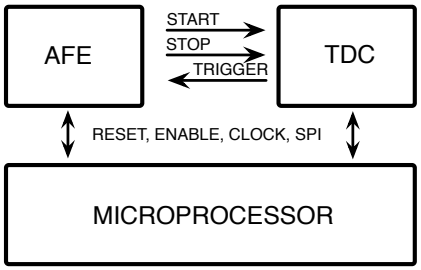

Fig. 2. Block diagram of the flow meter electronic system.

the proposed TDC and a microprocessor. The input of the TDC is a START and STOP pulse, the rising edges of which form the time interval to be digitized. When the microprocessor asks for a measure, the TDC generates a TRIGGER signal for the AFE and waits for a pulse back, the START signal. The AFE controls the ultrasound transducers and transmits N pulses at the main resonance frequency (1 MHz). Together with the first transmitted pulse, the START signal for the TDC is generated. The echo signal propagates through the liquid and reaches the paired transducer. The AFE amplifies the echo signal by means of a programmable gain amplifier cascaded to a low noise amplifier and generates the STOP pulse thanks to a zero-cross voltage comparator. The microprocessor provides to the AFE and the TDC the system master clock, the enable and the reset signals and communicates with the TDC through a serial peripheral interface.

As mentioned, the time interval T_{MEAS} from the rising edge of the START pulse to the rising edge of the STOP pulse is digitized in three parts, as conceptually shown in Fig. 3. The main part, T_{COARSE} is synchronous with respect to the system clock and is digitized by counting clock pulses with period T. The fractional parts, T_{START} and T_{STOP}, are digitized with two SAR-based converters, as it will be described in the next Section. In this way, T_{MEAS} is given by:

$$T_{MEAS} = T_{COARSE} + T_{STOP} + T - T_{START} \quad (2)$$

In order to save power, the TDC circuitry which measures the fractional parts is placed in sleep-mode after the digitalization of T_{START}. The circuit wakes up for the T_{STOP} measure after a given time, the expected time of flight (ETOF), a parameter provided to the TDC by the microprocessor during the power on and initialization phase.

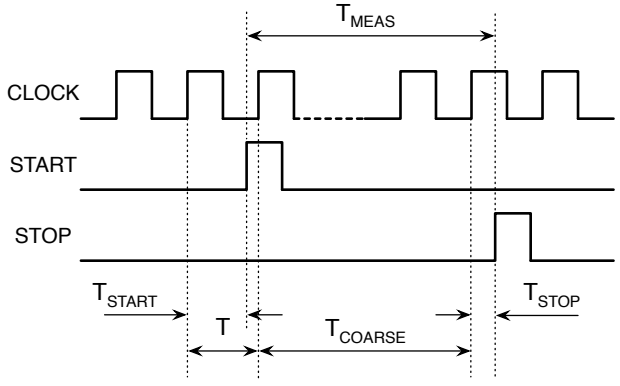

Fig. 3. Operating principle of the TDC.

III. TDC Design

The fractional measurements of the time of flight are performed with the scheme depicted in Fig. 4. It consists of two SAR ADCs, working alternatively, able to directly provide the time to amplitude conversion. During the period in which conventional SAR ADCs sample the input voltage, the proposed SAR ADC architecture charges the capacitors with a constant current ($I_{IN,A}$, $I_{IN,B}$). In the period in which channel A is charging the capacitors, channel B is in the discharge phase and vice-versa. At the rising edge of the START/STOP pulse, the current is stopped and the voltage is converted with the conventional SAR algorithm.

To meet the target system resolution, each SAR ADC has 12-bit resolution. The scheme uses a capacitive split-array consisting of a 6-bit main array, a 6-bit sub-array and a unity coupling capacitor, [9]. The solution saves silicon area and power consumption since the required capacitance is strongly reduced with respect to an equivalent conventional binary wighted array. In addition, the use of a unity coupling capacitor instead of the conventional fractional value improves the matching at the expense of only a small gain error.

The main challenges of this design are the need of an accurate constant current generator, of a proper strategy to handle the START/STOP detection when the pulse arrives close to the rising edge of the reference clock, and of advanced calibration techniques to meet the target resolution. The above issues are discussed in the following sub-Sections where the adopted design choices are described.

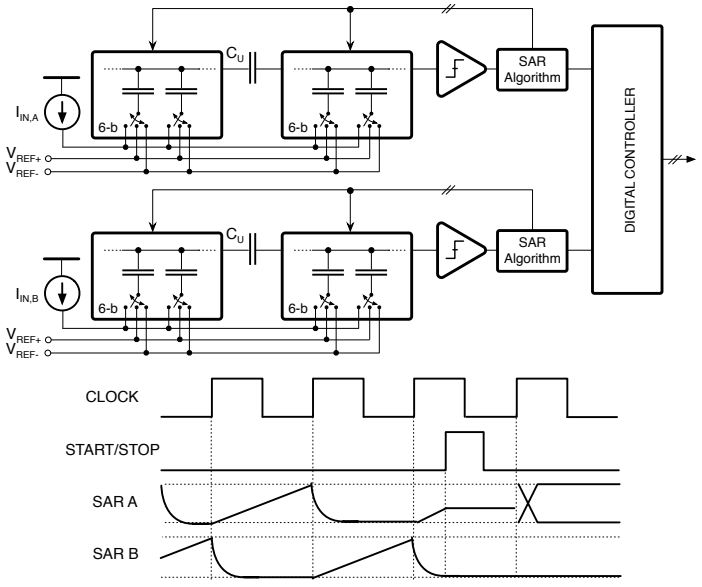

Fig. 4. Block diagram of the SAR-based ADC and simplified phases diagram.

A. Current Generator Design

Speed and accuracy requirements suggest to resort to the current steering technique for the current generator design. The basic current steering cell consists of a differential input pair driven by logic signals that switches a given current on two load resistances. The switched current is provided to the current steering cell by means of a simple or cascode current mirror. One of the limits of this circuit is the sensitivity to clock feedthrough and charge injection. When a MOS transistor switches on or off, a given amount of charge, corresponding to the charge trapped in the channel, is injected at the two sides of the channel. Moreover, there is an injection of charge caused by the capacitive coupling between gate and output node. This is particularly critical in our application since each non-linear error is translated in an error in the time measurement.

The schematic diagram of the current generator used in this design which overcomes the above drawbacks is shown in Fig. 5. The circuit is an improvement of the current steering cell used in [10]. The switching of the current (from branch composed by M_7, M_3, and M_2 to branch including M_5 and M_{10}) is performed by using only one large switching element, namely M_4. The circuit increases the output resistance of the cascode current mirror by mean of the amplifier boost M_3-M_{10}. This maintains the current charging the capacitor constant improving the linearity of the TDC. When the switch M_4 turns on, transistor M_3 turns off. The charge injected from M_3 and the charge trapped in the parasitic capacitors at the drain of M_3, that would flow to the capacitor, are drained to ground by means of minimum sized transistor M_1.

B. TDC Critical Decisions

The SAR ADCs driving phases diagram shown in Fig. 4 is not optimal when the START/STOP pulse arrives close to the rising edge of the system clock. Indeed, the required resolution is lower than the setup time of the D flip-flops available in the used technology: the risk is metastability. To face this issue, the solution is to adopt the phases shown in Fig. 6. The TDC uses a faster clock signal (32 MHz) available in the system to generate for the two SAR ADCs the clock signals

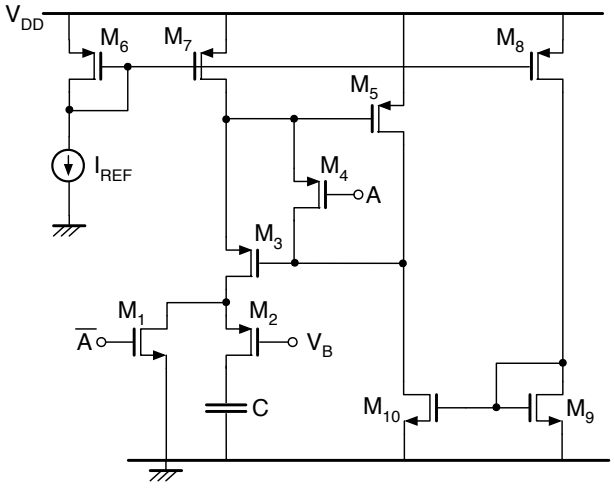

Fig. 5. Schematic diagram of the used current steering cell.

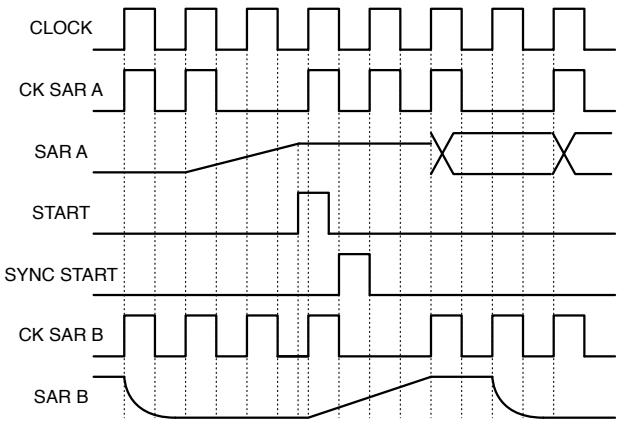

Fig. 6. Phases diagram for the proposed scheme.

at 16 MHz with 25% duty cycle with an extra pulse in the period immediately after the capacitor charge. These signals (CK SAR A and B in the figure) can be derived from the main clock with clock gating techniques. In this way, the charge on the capacitor array of the SAR is maintained while the START/STOP signal is synchronized with the first falling edge of the clock. The decision is postponed to the rising edge of the extra clock pulse: if the START/STOP pulse did not arrive, the SAR will discharge its capacitor array, otherwise the charge will be retained for the rest of the period and the conversion starts with the rising edge of the next regular clock pulse. The conversion is delayed by one clock period, but this latency is not a problem since the logic controlling the course clock counter properly accounts for the decision.

C. Offset and Gain Calibration

The TDC requires calibration. Indeed, switches charge injection critically affects the linearity of the generated currents $I_{IN,A}$, $I_{IN,B}$. To overcome this problem, the current generators are turned on and connected to the SAR capacitor arrays slightly before the rising edge of the main clock signal. This results in a fixed offset for the TDC that needs to be compensated for. In addition, possible gain errors have also to be taken into consideration.

Calibrations of the two SAR ADCs take place in the dead time between START and STOP fine measurements. In particular, when the microprocessor wakes up the TDC after the ETOF, the two SAR ADCs have time to calibrate gain and offset. The calibration process is as follows. First, the two SAR ADCs convert subsequently the full clock period, thus estimating possible gain errors in the fine measure. After that, the two SAR ADCs measure the offset and, when the SAR B concludes the last calibration, the TDC enters the read mode. The full scale and offset measures are provided to the microprocessor for proper signal processing. The TDC logic operations are controlled by a dedicated finite state machine.

IV. Simulation Results

The proposed TDC has been designed and fully simulated at the transistor level with a standard 0.13-μm CMOS technology. The nominal circuit supply voltage is 3.3 V and the

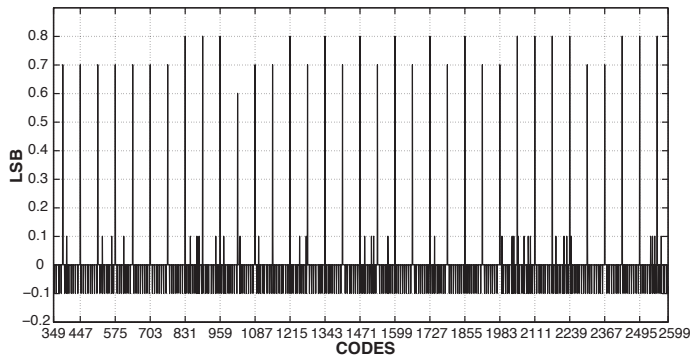

Fig. 7. Simulated TDC DNL.

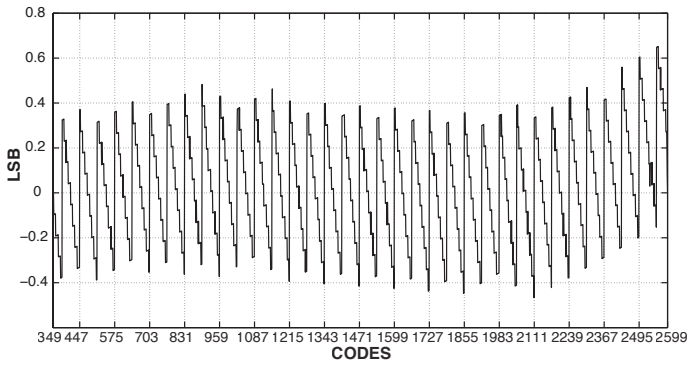

Fig. 8. Simulated TDC INL.

references used for the SAR ADCs are 0.8 V and 2.4 V. The nominal currents $I_{IN,A}$ and $I_{IN,B}$ are 150 μA.

The linearity of the proposed circuit has been simulated with 10 simulations for each code (START signal was maintained across all the simulations, while STOP signal has been delayed by $T_{lsb}/10$ at each step). The achieved DNL plot is given in Fig. 7: DNL is always negative, but there are cyclic positive peaks separated by 2^6 codes, where 6 is the number of elements of each sub-array of the capacitive DAC. This property of the DNL is typical for capacitive split-DACs and is caused by parasitics of the bridge capacitor: because these are generally different, the total capacitance of each array will be different, thus generating non linearity, [11]. This DNL gives the staircase-like curve of the INL shown in Fig. 8: the envelope of this curve is due to additional non-linearities of the circuit, besides the one ascribed to the split-DAC. In both curves, x-axis starts from 349, which is the value calibrated at the beginning of the period, and ends at 2599, the value calibrated at the end of the period. Values of DNL and INL beyond these limits are irrelevant for the application. The simulated DNL and INL values are within the intervals $[-0.1, 0.8]$ and $[-0.425, 0.625]$ LSBs, respectively. The simulated equivalent resolution is of about 27.8 ps.

The simulated current consumption for each SAR is 880 μA when all the blocks are active, but this value is reduced to 280 μA during conversion because the current generator ($I_{IN,A}$ or $I_{IN,B}$) is turned off. The power consumption averaged over the entire cycle of measure, taking into account the waiting time during which all the analog blocks are switched off, becomes lower. It depends on the expected time of flight (shorter the ToF and higher the mean power consumption) which can vary from 30 μs to 100 μs: with these values, the average power dissipated by each SAR ranges from 65 μW to 272 μW. Doubling these values, the total maximum TDC power dissipation can be estimated as 544 μW. Assuming a reasonable duty-cycle of 1 s for this type of measurements, the mean power consumption results in 26 nW.

V. Conclusion

This paper presented an hybrid course-fine TDC for flow metering applications in which the course measurement is performed in the digital domain while the fine measurement is achieved with two current-mode SAR ADCs. The presented architecture has been fully simulated at the transistor level with a 0.13-μm CMOS technology. Thanks to the use of an improved current steering cell, the converter is able to obtain about 27-ps resolution with a maximum power consumption of 544 μW.

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