A Single Op-Amp 0+2 Sigma-Delta Modulator

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Abstract—**This paper describes a single op-amp 0+2 $\Sigma\Delta$ architecture and design considerations to achieve 12-b resolution on a 2-MHz bandwidth. The proposed topology combines op-amp reduction and MASH techniques. In particular, the second-order $\Sigma\Delta$ stage uses direct synthesis of the noise transfer function (NTF) and employs only one op-amp. The use of multi-bit quantization on both stages increases the resolution of the modulator and reduces the output swing of the op-amp. The mismatch of the multi-level DACs can be compensated for with DEM while the mismatch between the two stages can be canceled in the digital domain. Simulation results, carried out at the transistor level with a 0.18-μm CMOS technology, verify the effectiveness of the proposed architecture. The simulated FoM is 104 fJ/conv-step.**

I. Introduction

Sigma-Delta modulators ($\Sigma\Delta$Ms) are popular in the field of analog-to-digital conversion. Thanks to oversampling and noise shaping, $\Sigma\Delta$Ms are able to tolerate circuit imperfections and thus relaxing strict requirements on analog components, [1]. Discrete-time (DT) $\Sigma\Delta$M architectures represent a good choice for applications with high resolution ($\geq$12b) and medium-low bandwidth ($\leq$2 MHz). In such cases, low-power dissipation is the key parameter since those modulators are always used in power-demanding electronic systems, [2].

To achieve low-power dissipation, the op-amp reduction technique has been a popular choice for various designs, [3][4]. The work reported in [3] presents a second-order $\Sigma\Delta$M with single op-amp implementation and double sampling. A third-order $\Sigma\Delta$M realized by using only one op-amp has been reported in [4]. The circuit was able to achieve about 14-b resolution with a figure of merit (FoM) as low as 54 fJ/conv-step. Nonetheless, for those single-stage $\Sigma\Delta$Ms, stability requirements may degrade the achievable resolution when the order of the $\Sigma\Delta$M is higher than two. To overcome this limitation, the multi-stage topology (MASH) has been addressed, [5][6]. These kind of architectures are particularly effective for high order and low oversampling ratio (OSR) because of enhanced stability and better signal-to-noise and distortion ratio (SNDR) performance when compared with the equivalent single-stage counterparts. In particular, the 0+$\Sigma\Delta$ architecture, [6], demonstrated its stability with a input signal level larger than any conventional topology. However, the modulator proposed in [6] uses three op-amps to implement a third-order noise transfer function (NTF) and the power efficiency is unsatisfactory.

This paper presents a $\Sigma\Delta$ architecture which combines the
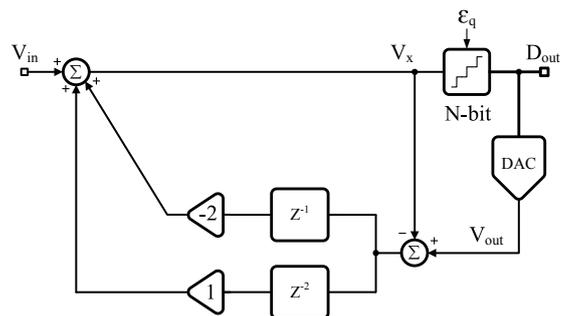

Fig. 1. Single-stage second-order $\Sigma\Delta$ topology block diagram.

op-amp reduction and MASH, [5], techniques. It is a 0+2 $\Sigma\Delta$ topology utilizing only one op-amp and direct synthesis of the NTF in the second-order $\Sigma\Delta$M stage. The power consumption is diminished for two main reasons: 1) the reduced number of op-amps used in the modulator; 2) MASH architecture and multi-bit quantization ensure the stability and keep the output swing of the single op-amp minimized. The proposed circuit, simulated at the transistor level with a 0.18-μm CMOS technology, achieves 12-bit resolution over 2-MHz bandwidth consuming 1.7 mW.

II. Proposed Architecture

This Section describes first the proposed second-order $\Sigma\Delta$M scheme which features direct synthesis of the NTF and that uses only one op-amp in its implementation. This scheme is then combined with an additional input stage consisting of an M-bit quantizer to achieve the final 0+2 scheme with charge reuse.

A. Single-Stage Second-Order $\Sigma\Delta$ Topology

Fig. 1 illustrates the block diagram of the proposed second-order scheme. It consists of an N-bit quantizer and DAC, two analog delay paths with proper coefficients and delays and two analog summation nodes. The circuit works as follows: the quantization error ϵ_q is estimated by the difference between V_{out} (ideal analog value of D_{out}) and V_X, as indicated in Fig. 1. The quantization error goes through two different analog delay paths and is added to the input signal V_{in}. The result is V_X. By inspection of the circuit, the transfer function in z-domain can be calculated as:
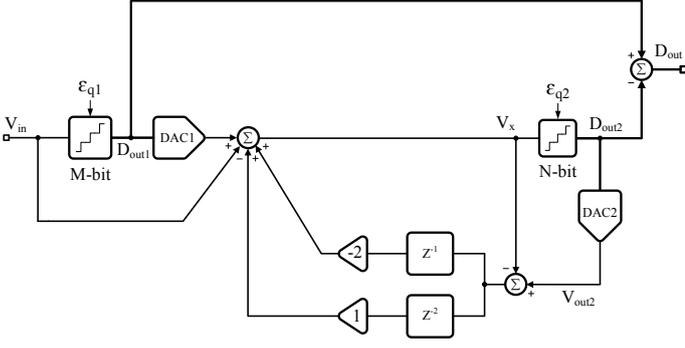
Fig. 2. 0+2 ΣΔ scheme block diagram.

$$D_{out}(z) = V_{in}(z) + (1 - z^{-1})^2 \epsilon_q(z) \qquad (1)$$

where the quantization error $\epsilon_q(z)$ is shaped by a second-order high-pass NTF. The main benefit of the topology is that it obtains a second-order noise shaping without any integrator in the loop filter. This may leads to lower power dissipation in the circuit implementation.

However, a few issues deserve further discussion. The requirements for realizing an accurate analog adder at the input of the modulator represent a first limit. Indeed, in order to achieve 12-b resolution, an accuracy of 0.1% should be guaranteed. Such an high accuracy can be only achieved by means of an high gain op-amp. Secondly, the voltage swing of V_X is large, as can be seen in the following z-domain expression:

$$V_X(z) = V_{in}(z) + (z^{-2} - 2z^{-1})\epsilon_q(z) \qquad (2)$$

The voltage swing at V_X is as large as V_{in} and may result in an analog adder consuming considerable power if realized with an op-amp.

B. 0+2 ΣΔ Scheme

To overcome the above mentioned limitations, consider the 0+2 topology scheme of Fig. 2. It illustrates the block diagram of the proposed 2-stage ΣΔ ADC. The first stage uses an M-bit quantizer to digitize V_{in} and generates a coarse digital output, D_{out1}. The input of the second stage, the quantization error of the first stage, ϵ_{q1}, is processed by the second-order ΣΔ scheme of Fig. 1. The quantization error of the second stage, ϵ_{q2}, is shaped by the second-order high pass NTF and the digital output is D_{out2}. The combination of D_{out1} and D_{out2} cancels out ϵ_{q1} and generates the final digital output of the modulator D_{out}. The transfer function is:

$$D_{out}(z) = V_{in}(z) - (1 - z^{-1})^2 \epsilon_{q2}(z) \qquad (3)$$

The scheme of Fig. 2 allows reducing the swing of V_X when compared to the scheme of Fig. 1. Thus, the requirements of the op-amp used to realize the analog adder are relaxed and the power consumption can be reduced.
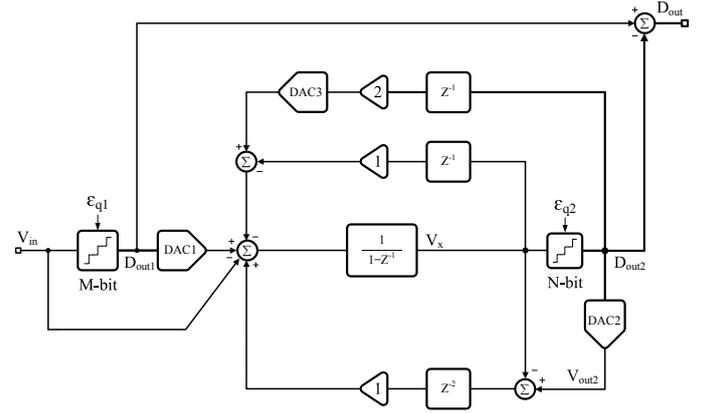

Fig. 3. 0+2 ΣΔ scheme with charge reuse.

C. 0+2 ΣΔ with Charge Reuse

When using an op-amp based analog adder at the input of the scheme of Fig. 1, after the summation operation in each clock period, in order not to disturb the operation in the following clock cycle, the voltage at the output of the op-amp should be erased. This requires to introduce a reset clock phase which slows down the speed of the whole modulator.

This limit can be overcome by rearranging the scheme of Fig. 2 by rewriting the expression of $-2z^{-1}\epsilon_{q2}(z)$ as follows:

$$\begin{aligned} -2z^{-1}\epsilon_{q2}(z) =& -2z^{-1}\{V_{out2}(z) - V_X(z)\} \\ =& z^{-1}V_X(z) + z^{-1}\{V_X(z) - 2V_{out2}(z)\} \end{aligned} \qquad (4)$$

From (4), notice that the voltage V_X can be reused in the following clock period and does not need to be erased. Indeed, at the end of *n-th* clock period, the output of the analog adder is $V_X(n)$. In the following clock period, the analog branch $-2\epsilon_{q2}(n)$ is added to V_{in} and $V_X(n+1)$ is generated. Hence, there is no need to erase $V_X(n)$ while $2V_X(n)$ is required during the $(n+1)$-th clock period. In order to keep unchanged the modulator transfer function and avoid introducing a reset phase, the feedback signal $-2\epsilon_{q2}(n)$ can be replaced with $V_X(n) - 2V_{out2}(n)$ and the analog adder can be substituted with an integrator without delay. Fig. 3 shows the final block diagram of the proposed 0+2 scheme.

III. Design Considerations

This Section discusses the different design challenges to be faced while targeting a resolution of 12-bit over a signal bandwidth of 2 MHz with the architecture of Fig. 3: effects of finite gain and bandwidth of the integrator, mismatch between the two stages and mismatch among the unity elements of the multi-level DACs. To achieve the target resolution and bandwidth, this design uses M = 3, N = 5 and OSR = 16.

A. Op-Amp Performance

Let us first study the limits caused by the finite gain of the op-amp. As known, when using an op-amp as an integrator, the finite gain causes a leakage and only a fraction of the previous output sample is added to the current input sample.
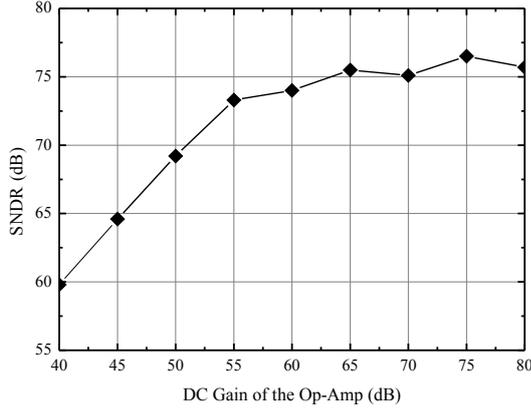
Fig. 4. Simulated SNDR as a function of the DC gain of the op-amp.

This effect is studied at the behavioral level. The input of the modulator is a -3 dB$_{FS}$ sinusoid waveform with a normalized frequency equal to 0.0021. The integrator is modeled with the toolbox proposed in [7]. Fig. 4 shows the achieved SNDR as a function of the DC gain of the op-amp. For 12-bit resolution, the minimum required DC gain is 60 dB.

Besides the DC gain, another important design parameter is the op-amp bandwidth. When targeting low input signal bandwidth, the architecture shown in Fig. 3 requires to satisfy op-amp bandwidth specifications generally not difficult to meet. Nevertheless, when the input signal bandwidth is in the MHz range, the settling behavior imposes large gain-bandwidth (GBW) products, thus degrading the power efficiency of the modulator. This design limits the problem with a three-phases operation, that will be described in the following subsection.

B. Circuit Implementation and Three-Phases Operation

Fig. 5 shows the fully differential schematic diagram of the 0+2 modulator (for the sake of simplicity, the single ended analog delay lines scheme is given) together with its driving phases. The circuit consists of one op-amp, two quantizers, two DACs and related digital controls. ADC1 is a 3-bit flash which converts the input signal by using eight comparators. ADC2 is a 5-bit flash. Since the output swing of the op-amp is less than $0.2V_{ref}$, ADC2 uses only eight comparators. The combination of the digital outputs D_{out1} and D_{out2} generates the final output D_{out} (combination logic not shown in Fig. 5). Different analog delay lines are implemented with switched-capacitors (SC) circuits.

Conventional implementations of DT ΣΔMs use SC circuits working in two-phases. Realizing the scheme of Fig. 3 with the conventional two-phases approach would lead to a feedback factor, β_{2ord}, of the op-amp equal to 1/5. This parameter needs to be optimized in order to improve the settling speed of the amplifier. In this respect, this design uses a three-phases
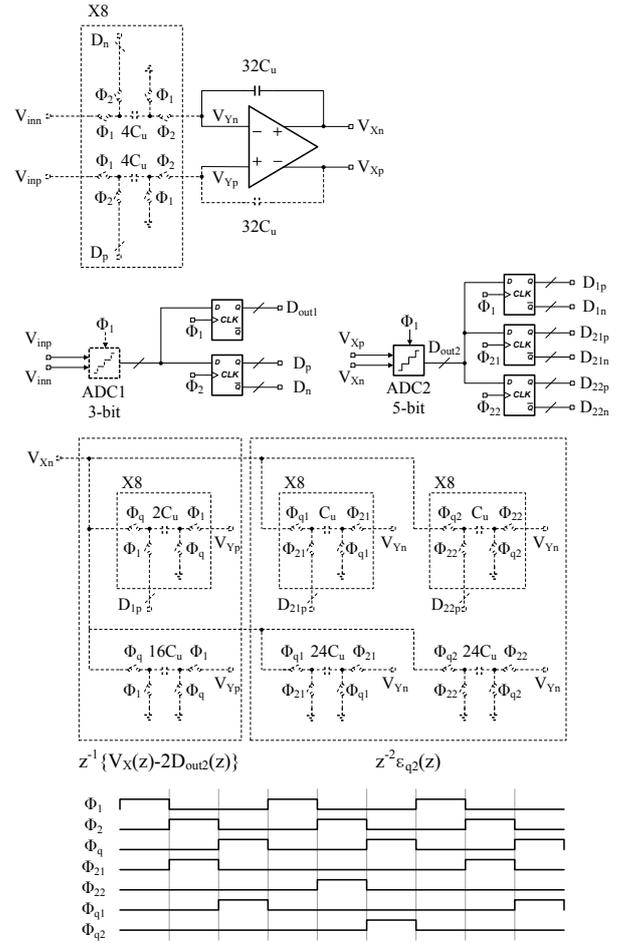

Fig. 5. Schematic diagram of the proposed 0+2 ΣΔ architecture with driving phases.

approach: a full clock period is divided into three equal phases so that the analog summation can be divided into two parts and operated in two successive clock phases. Tab. I summarizes the operations performed in each phase. During ϕ_1, $\epsilon_{q1}(z)$ charges the input sampling capacitor while $z^{-1}\{V_X(z)-2V_{out2}(z)\}$ injects its charge. During ϕ_2, both $\epsilon_{q1}(z)$ and $z^{-2}\epsilon_{q2}(z)$ inject the charge on the integrator. At the end of ϕ_1 and ϕ_2, the new value of V_X is ready. In ϕ_q, this value is used to charge the two analog delay lines which will be utilized in the next clock period. At the same time, the quantizer converts V_X and determines the digital output D_{out2}. With the three-phases operation, β_{2ord} is equal to 1/3 thus significantly improving the situation with respect to the conventional two-phases approach.

C. Mismatch Between Two Stages

A mismatch between the two stages (i.e., the input flash and the ΣΔM) will degrade the performance and needs to be studied. Suppose a gain error $(1+\epsilon_G)$ is at the input of the second stage: the digital output of two stages are described by the following equations:

$$D_{out1}(z) = V_{in} + \epsilon_{q1}(z)$$
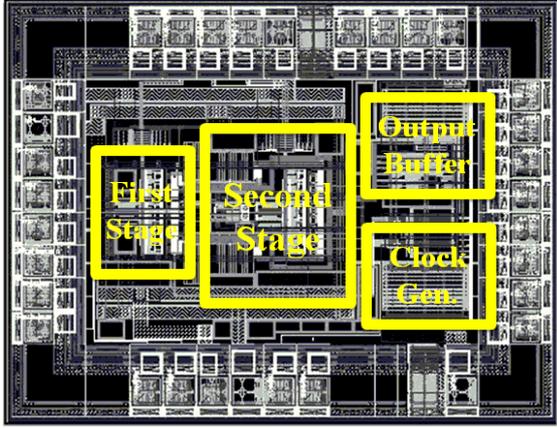$$D_{out2}(z) = \epsilon_{q1}(z)(1 + \epsilon_G) - (1 - z^{-1})^2\epsilon_{q2}(z) \quad (5)$$

TABLE I. PHASES AND OPERATIONS.

	ϕ_1	ϕ_2	ϕ_q
$\epsilon_{q1}(z)$	Charge	Inject	–
$z^{-2}\epsilon_{q2}(z)$	–	Inject	Charge
$z^{-1}\{V_X(z) - 2V_{out2}(z)\}$	Inject	–	Charge

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Fig. 6.   Layout of the proposed 0+2 ΣΔ modulator.

Fig. 7.   Simulated output spectrum of the proposed 0+2 ΣΔ scheme.

Using (5), the modulator output becomes:

$$D_{out}(z) = V_{in} - \epsilon_G \epsilon_{q1}(z) - (1 - z^{-1})^2 \epsilon_{q2}(z) \qquad (6)$$

where the quantization error of the first stage is not fully cancelled. The leakage of $\epsilon_{q1}(z)$ severely degrades the modulator performance. The problem can be solved by means of a digital calibration. By using the same gain factor $(1+\epsilon_G)$ to multiply D_{out1}, as shown in the following equation, the term $\epsilon_G \epsilon_{q1}(z)$ is canceled out. The exact value of ϵ_G is unknown in a real circuit, but the estimation of ϵ_G in the digital domain to obtain the optimum performance is a feasible method.

$$\begin{aligned} D_{out}(z) &= D_{out1}(z)(1 + \epsilon_G) - D_{out2}(z) \\ &= V_{in}(1 + \epsilon_G) - (1 - z^{-1})^2 \epsilon_{q2}(z) \end{aligned} \qquad (7)$$

D. Mismatch of Multi-Bit DACs

Non-linearity caused by the mismatch among the unity elements of the used multi-level DACs needs to be carefully studied. However, although the presence of four multi-bit DACs, conventional DWA algorithms, [2], can compensate for their mismatch effects. The issue has been studied at the simulation level. Four groups of mismatch (one for each DAC), obeying to a normal distribution with zero mean and $\sigma = 1\%$, have been employed. Simulation results show that, with a -3 dB$_{FS}$ input sinusoid waveform with normalized frequency equal to 0.0021, the achieved SNDR can improve from 51.3 dB (case with no DEM) to 76.7 dB (ENOB = 12.4b), which is almost equal to the value obtained with an ideal model.

IV.   Simulation Results

The proposed single op-amp 0+2 ΣΔ ADC has been designed with a 0.18-µm CMOS technology. The nominal supply voltage is 1.8 V. The unity capacitor C_u (MIM type) is 7.5 fF. The input sampling capacitor, C_S, is $32C_u$, 240 fF. To ensure high gain and high bandwidth with relatively low output swing, the used op-amp is a gain-boost telescopic scheme. Simulation results show that the DC gain and GBW of the main op-amp are 102 dB and 1.2 GHz, respectively, with a 480-fF load. Four DEM modules (DWA method) are used to compensate for the mismatch of the DACs. Their implementation requires about 1000 gates. Fig. 6 shows the la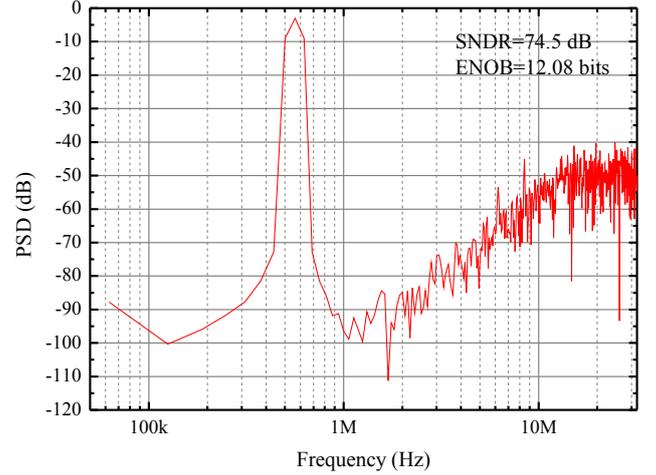yout of the full chip with main blocks highlighted. The active area is A = 860 x 600 µm² (the chip area is 1240 x 970 µm²). The area of the DEM modules is only 5%A.

The performance of the proposed 0+2 scheme is verified by transistor level simulations. Fig. 7 illustrates the PSD (1024-point FFT) of D_{out} when a -3-dB$_{FS}$ sinusoid waveform at 562.5 kHz is applied. The achieved SNDR is 74.5 dB, which is equal to 12.08 bit of resolution. The estimated power consumption is 1.7 mW leading to a Figure of Merit equal to 104 fJ/conv-step.

V.   Conclusions

In this paper a 0+2 ΣΔ architecture realized with a single op-amp featuring 12-bit of resolution over 2-MHz bandwidth has been presented. The scheme combines op-amp reduction and MASH techniques to limit the power consumption while keeping stability. Multi-bit quantization ensures low output swing of the single op-amp and three-phases operation allows affordable op-amp gain and bandwidth values. Simulation results at the transistor level verify the effectiveness of the approach.

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