Design of an Op-Amp Free Voltage Reference with PWM Regulation

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***Abstract*—This paper presents the design of an op-amp free voltage reference generator which utilizes a pulse width regulated loop. The proposed voltage reference circuit has been designed and simulated in a standard 0.18-μm CMOS technology. Post layout simulation results show that it is capable of operating with supply voltages down to 0.7 V while generating an output voltage of 202 mV. The achieved temperature coefficient is 54 ppm/°C for temperatures ranging from 0 to 100 °C. The simulated power consumption at the room temperature is 400 nW.**

I. Introduction

Voltage references are one of the critical building blocks of many systems on chip (SoCs) and mixed-signal integrated circuits (ICs) such as data converters and voltage regulators since they constitute a stable operating point for the rest of the system in order to generate predictable and repeatable results. Besides being insensitive to temperature, process and supply voltage variations, due to the increasing market demand for battery-operated circuits, ultra-low power consumption and capability to work with very low supply voltage levels have become the most stringent performance parameters for a high performance voltage reference circuit.

Historically, bandgap references (BGRs) have been the most popular solution to generate integrated precision references, [1]. Nowadays, however, the technology scaling and the aforementioned requests of low power and of more and more reduced supply voltage levels make traditional BGR architectures no more suitable for sub-1V operation. Two are the main reasons. The first one is that the BGR output voltage is equal to the extrapolated bandgap voltage of silicon at 0 K, ≈ 1.2 V, that exceeds 1 V. The second limit is posed by the required input common mode voltage level of the amplifier used in the feedback loop that generates the proportional to the absolute temperature (PTAT) current in conventional solutions, [2], [3].

Different approaches have been proposed to overcome these two problems. One of them, [2], uses a resistive subdivision method that allows scaling down the reference voltage in the output branch in order to eliminate the first problem. These circuits are referred as current-mode references since they generate a temperature-independent current, which is then mirrored to an output resistor to create a sub-1V output voltage. However, even if the theoretical usable minimum supply voltage for this architecture is $V_{DD,min} = V_{EB} + |V_{DS\,sat,p}|$, practically, the required minimum supply voltage is limited by the input common mode range of the op-amp used to generate the PTAT current. To overcome this limitation, several techniques have been published: among them, the use of native (low-threshold) devices, [2], the use of a BiCMOS technology, [4], the use of an amplifier with PMOS input stage driven by a potential divider and with PMOS source-bulk junctions partially forward biased to reduce their threshold voltage, [5], the use of dynamic threshold MOS (DTMOS) devices, [6].

Increasing requirements for reference generators working with very low supply voltage and very low power should be satisfied by new circuit solutions using standard technologies. This work presents the design of an op-amp free voltage reference. The proposed scheme offers a double benefit: it gets rid of the most power hungry block in voltage reference circuits and naturally solves the aforementioned limit imposed by the op-amp input common mode range. The proposed voltage reference circuit uses a reverse current-mode scheme and is regulated with pulse width modulation (PWM). The circuit, designed and simulated at the post layout level with a 2-poly, 6-metal, standard 0.18-μm CMOS technology, achieves an output voltage of 202 mV with a temperature coefficient

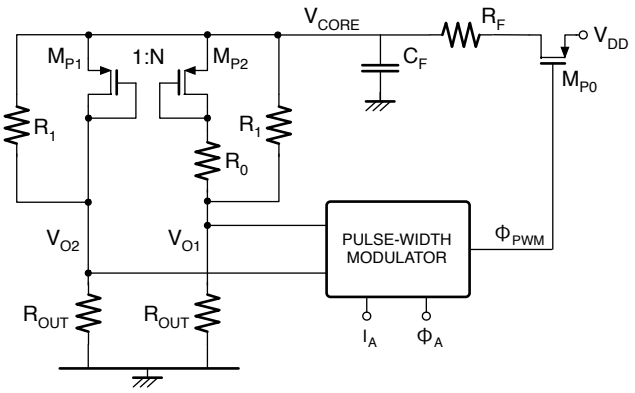

Fig. 1. Schematic diagram of the proposed voltage reference architecture.

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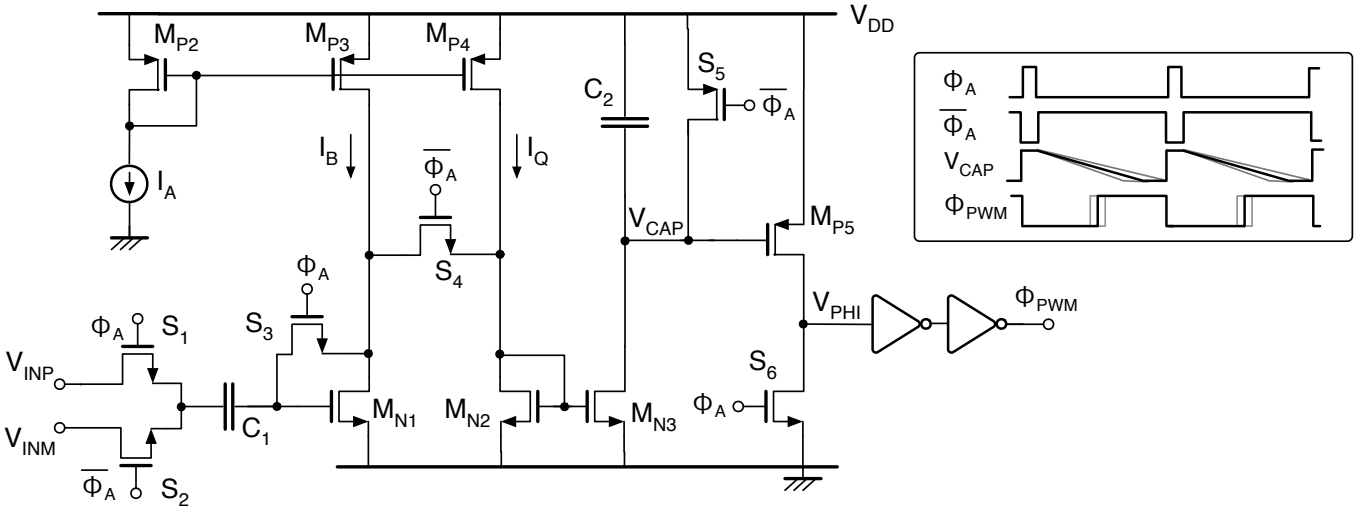

Fig. 2. Schematic diagram of the pulse-width modulator.

(TC) of 54 ppm/°C in the temperature range 0 − 100 °C and consumes always less then 500 nW over the entire temperature range with a supply voltage as low as 0.7 V.

II. Proposed Voltage Reference

Fig. 1 shows the schematic diagram of the proposed voltage reference circuit. The conventional current mode bandgap, [2], is reversed so that the reference voltage is generated across the output resistors R_{OUT}. The direct transformation of PTAT and CTAT currents into voltage with a reversed architecture avoids the use of current mirrors, often source of inaccuracy, [7]. Transistors M_{P1} and M_{P2} operate in the sub-threshold region to provide the diode-like voltage-current response, as required to give rise to PTAT and CTAT currents. The PMOS switch M_{P0}, digitally driven by the pulse-width modulator block, generates the voltage V_{CORE}. The action of the simple RC network (composed by R_F and C_F) adequately filters out the ripple caused by the PWM on V_{CORE}. The loop equates the two output voltages, V_{O1} and V_{O2}. The output voltage of the circuit can be expressed as

$$V_{O1,O2} = \frac{R_{OUT}}{R_1}\left[V_{GS1} + \frac{R_1}{R_0} n V_T ln\,(N)\right] \tag{1}$$

With $N = 16$ and $R_1/R_0 = 2.25$, it is first order temperature independent. R_{OUT} is chosen equal to 1 MΩ to have an output voltage of 200 mV. The operation incorporates the start-up function, which is always required in bandgap circuits.

A. Pulse-Width Modulator

Fig. 2 shows the schematic diagram of the designed pulse width modulator. There are two phases of operation. In the first phase, Φ_A, the input transistor, M_{N1}, is connected in the diode configuration to charge the auto-zero capacitor C_1 to V_{INP} minus the V_{GS} of the input transistor itself. In the second phase, $\overline{\Phi_A}$, the signal current, i_d, flows through the switch S_4 into M_{N2} and is mirrored to M_{N3} in order to charge the capacitor C_2, initially discharged in the auto-zero phase. In this phase, the voltage V_{CAP} linearly decreases and the V_{GS} of M_{P5} is compared with the threshold voltage of M_{P5}. The result at the node V_{PHI} is a square wave, which is enforced by a tapered inverter chain to generate the PWM signal at the output. Fig. 2 conceptually shows the operation and provides the phases diagram and the evolution of the voltage V_{CAP}. The input differential voltage and the transconductance of the input transistor M_{N1}, which operates in the sub-threshold region, give rise to the charging signal current:

$$i_d = g_{m,MN1}\,(V_{INP} - V_{INM}) = \frac{I_B}{nV_T}\,(V_{INP} - V_{INM}) \tag{2}$$

where I_B is the bias current of M_{N1}, n the sub-threshold region slope and V_T the thermal voltage.

The quiescent pulse width, PW_Q, of the generated square wave depends on the quiescent current, I_Q, the threshold voltage of M_{P5}, $V_{th,p,M5}$, the value of C_2, the auto-zero duration time, T_A, and the master clock period, T ($T_A < T$). With zero signal current, PW_Q is equal to

$$PW_Q = T - T_A - \frac{C_2|V_{th,p,M5}|}{I_Q} \tag{3}$$

In the preferred implementation, the bias current I_A is 10 nA and M_{P2} has W/L equal to 4. The aspect ratios of transistors M_{P3} and M_{P4} are 40 and 8, respectively, to achieve the nominal currents I_B and I_Q equal to 100 nA and 20 nA. The capacitor C_1 used for storing the input offset during the auto-zero period is 2 pF. The clock frequency is 100 kHz (T = 10 µs) with auto-zero phase, Φ_A, equal to 25% of the clock period (T_A = 2.5 µs). From (3), in order to achieve $PW_Q = (T - T_A)/2$, considering $|V_{th,p,M5}|$ = 0.45 V and C_2 = 0.15 pF, the quiescent current, I_Q, turns out to be equal to 18 nA. Table I gives the

TABLE I
TRANSISTOR SIZES OF THE PULSE WIDTH MODULATOR

Transistor	W/L
M_{P2}	20 µm / 5 µm
M_{P3}	200 µm / 5 µm
M_{P4}	40 µm / 5 µm
M_{P5}	50 µm / 0.18 µm
M_{N1}	100 µm / 1 µm
M_{N2}, M_{N3}	20 µm / 1 µm
S_1, S_2	0.22 µm / 0.18 µm
S_3, S_4, S_5, S_6	1 µm / 0.18 µm

transistors sizes of the designed circuit in the used 0.18-µm CMOS technology.

B. Supply Voltage Limit

The required minimum supply voltage for the proposed circuit depends on the desired output level and a number of practical limits. From Fig. 1, the minimum V_{DD} can be expressed as

$$V_{DD} = V_{O1,\ O2} + |V_{GS,MP1}| + V_F \tag{4}$$

where V_F is the voltage drop on the filter resistor when transistor M_{P0} is on. In our design, an output voltage of 200 mV, 400 mV across the PMOS diode at 0 °C (worst case for the target temperature range), and a voltage drop as low as 50 mV across R_F result in a minimum supply voltage equal to 0.65 V.

On the other hand, proper operation for switches S_1 and S_2 of Fig. 2 has to be ensured in order to avoid significant circuit performance degradation. This leads to the following additional constraint:

$$V_{DD} = V_{O1,\ O2} + V_{th,n} + V_{DS\,sat} \tag{5}$$

In the used technology, the threshold of the N-channel transistors is 450 mV at 0 °C (that is the worst case for the target temperature range). Hence, with an overdrive voltage of 50 mV, the minimum required supply voltage becomes 0.7 V. However, this constraint can be eliminated if the driving signals of the two switches are properly boosted, for instance by means of simple voltage doubler circuits, [8].

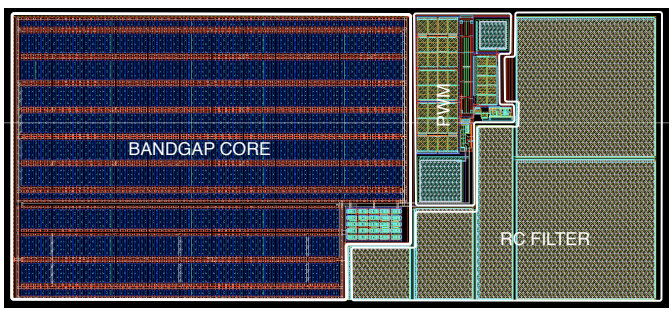

Fig. 3. Layout of the proposed voltage reference circuit.

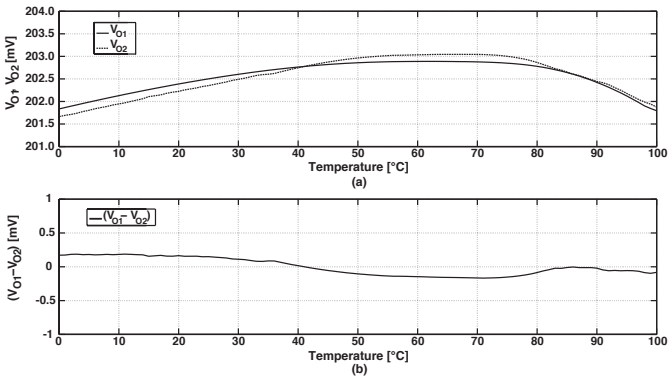

Fig. 4. Post layout simulation of (a) the two output voltages and (b) of their difference as a function of the temperature.

III. SIMULATION RESULTS

This voltage reference has been designed and simulated at the post layout level in a standard 0.18-µm CMOS technology with 6 metal and 2 poly layers. Fig. 3 shows the layout of the circuit with main blocks highlighted. The circuit occupies an active area of 370 µm × 170 µm that is mainly dominated by the resistors used in the bandgap core and by the capacitor of the RC filter. The nominal supply voltage and the master clock frequency are 0.7 V and 100 kHz, respectively. The auto-zero phase, Φ_A, is set to 25% of the master clock period.

Fig. 4 shows the two output voltages and their difference as a function of the temperature. The circuit generates two output voltages of about 200 mV in the nominal process corner. In the temperature range from 0 °C to 100 °C, the difference between the two outputs is less then ± 0.5 mV. For this temperature range, the achieved TCs of the outputs, V_{O1} and V_{O2}, are 54 ppm/°C and 62.5 ppm/°C, respectively.

Fig. 5 plots the distribution of the output voltage levels for the two outputs obtained through 100 process and mismatch Monte Carlo simulation runs without any device trimming or current calibration for the PWM circuit. The mean values of the two output voltages are ≈ 202 mV with standard deviations of 1.665 mV and 1.717 mV, respectively.

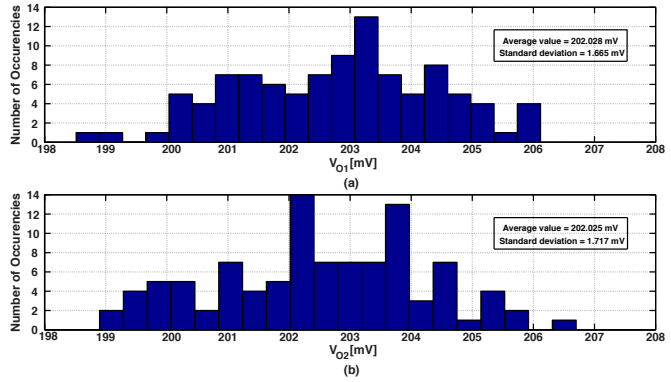

Fig. 5. Untrimmed output voltages level distribution achieved with 100 Monte Carlo simulation runs. (a) V_{O1}; (b) V_{O2}.

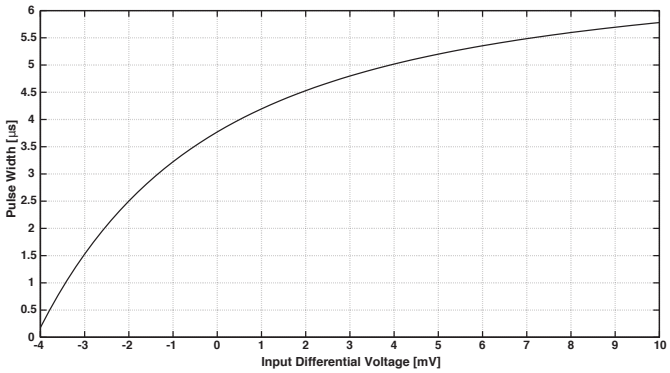

Fig. 6. Post layout simulation of the PWM signal pulse width as a function of input differential voltage.

Fig. 6 gives the pulse width of the generated PWM signal as a function of input differential voltage (input-output characteristic of the PWM circuit). Note that, with a negative input signal, the current charging the capacitor C_2 diminishes, thus increasing the time required to the voltage V_{CAP} for crossing the value $V_{DD} - |V_{th,p,MP5}|$. The pulse width of the generated signal on node V_{PHI} (and, consequently, Φ_{PWM}) decreases. A positive input signal, on the contrary, speeds up charging C_2 and the pulse width of the output signal becomes larger.

Fig. 7 shows the quiescent pulse width of the PWM signal, PW_Q, as a function of the temperature in the range from 0 to 100 °C. The positive slope of the curve is caused by two effects, both ascribed to the transistors threshold temperature dependence. The first and dominant one is the threshold voltage variation of M_{P5}, that decreases the charge needed on capacitor C_2, hence, increasing the output pulse width. The second effect is the variation of the threshold of the transistors composing the current mirrors (M_{P3}-M_{P4} and M_{N2}-M_{N3}) which provide the quiescent bias current. The latter increases with temperature.

Fig. 8 shows the supply current as a function of the temperature when the nominal supply voltage is 0.7 V. The supply current is increasing with temperature because of the CTAT behavior of the V_{GS} of PMOS transistors, M_{P1} and M_{P2}. The average value of the supply current is 590.5 nA. At room

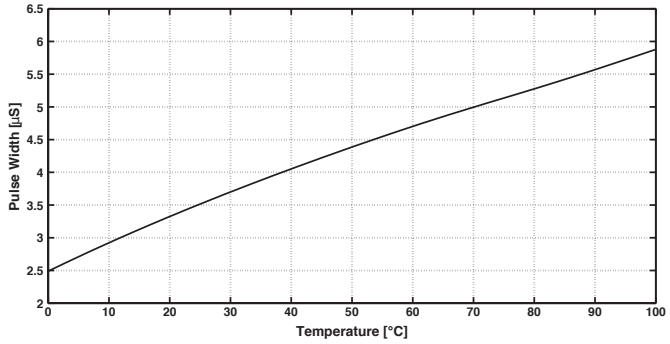

Fig. 7. Post layout simulated pulse width variation as a function of temperature.

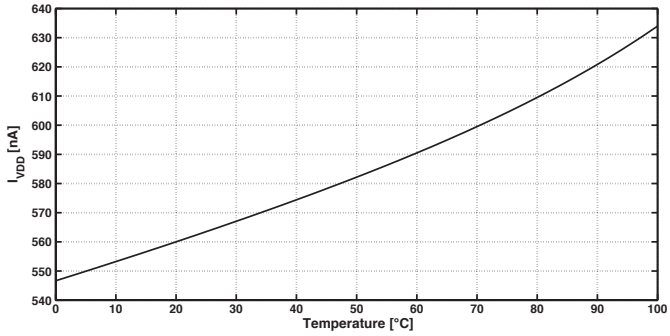

Fig. 8. Supply current variation as a function of temperature simulated at the post layout level.

temperature, the supply current is about 565 nA, thus bringing the power consumption to 395.5 nW. Even for the worst case (at 100 °C), the power consumption is less then 0.5 μW.

IV. Conclusion

This paper presented a novel low power voltage reference circuit implemented without any operational amplifier. The circuit is regulated with pulse width modulation. The scheme, designed and simulated at the post layout level with a standard 0.18-μm CMOS technology without any special process step, is capable of operating with very low supply voltage and achieves a temperature coefficient of 54 ppm/°C in the temperature range 0 – 100 °C. The simulated power consumption is always less than 500 nW.

Acknowledgment

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