A Capacitive Sensor Interface for High-Resolution Acquisitions in Hostile Environments

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***Abstract*—This paper presents a novel architecture for capacitive sensor interfaces that is insensitive to electro magnetic interferers in hostile environments. A bridge structure, with a feedback control and a special band-pass filter, overcomes the problems that affect the standard approaches. Behavioural level simulations demonstrate the feasibility of the idea for 12-bit resolution.**

Keywords—EMI-Free Acquisition, N-Path Filter, Capacitive Sensor, ADC.

I. Introduction

The growing capacitive sensors market asks for reliability and robustness. Applications involve a wide variety of sensing and measurement situations such as proximity detection, linear and rotary position encoding, fluid level determination, pressure measurements, acceleration sensors and so on. The accuracy of capacitive sensors is excellent. Furthermore, sensors can be integrated in a silicon substrate thus ensuring miniaturisation and integration with the sensor interface.

The capacitance measurement can be directly performed together with the analog to digital conversion, [1], [2]. Typically a sampled data $\Sigma\Delta$ or an incremental converter incorporates the capacitive sensing element in the input stage. This method works properly in protected environments, but it becomes problematic when the environment where the sensor is placed is hostile. Electromagnetic interferers (EMI) corrupt the sensor signal, and their processing leads to tones that the converter intrinsic non-linearities might fold into the band of interest. The result is a measurement error with an amplitude that may degrade the overall accuracy.

The measurement of capacitances using high frequency sine waves and a possible frequency hopping addresses the problem, [3]. However, interferences with high amplitude can saturate the active elements of the interface even if the frequency distance between the signal and the EMI is large.

The method proposed by this paper faces the above limit. It avoids the use of virtual grounds on the input path; after a suitable passive processing that rejects a great part of interfering signals, the signal is applied directly to the input of an A/D converter for providing the measurement in digital format and closing a feedback loop.

II. Conventional measurement Method

Fig. 1(a) shows a typical acquisition chain for the measurement of capacitance variations. The buffered version of a synthesised sine wave drives one terminal of the capacitive sensor, C_s. The generated sinusoidal current enters the virtual ground of the op-amp and determines a sinusoidal output voltage whose amplitude depends on the ratio C_f/C_s. Mixing the output with the driving signal brings the result at DC for a successive analog low pass filtering and A/D conversion. A programmable gain amplifier in front of the ADC optimises the system signal-to-noise-ratio (SNR).

Notice that a leakage current entering or exiting the virtual ground node saturates the output. Moreover, a large interfering signal integrated over C_f may saturate the output, especially when, in order to increase the sensitivity, the value of the capacitance C_f is low and the charge injected by C_s is partially compensated by an auxiliary injecting network (Fig. 1(b)).

Unfortunately, since the EMI signal can stay in a wide range of the frequency spectrum, filtering is not effective to remove it at the beginning of the processing chain. Suppose to have a spur sine wave signal with amplitude A_{sp} and frequency f_{sp} coupled with the parasitic capacitance C_p to the virtual ground (Fig. 1(b)). The signal shows up at the output multiplied by C_p/C_f, a value that can be large for $C_p >> C_f$. This hostile signal is actually filtered but this happens only after the demodulator. Therefore, the gain C_f/C_s must be kept low with a consequent limitation of the overall dynamic range.

III. This Method

The basic idea behind the method used here is to balance the charge induced into the capacitance under measurement instead of integrating the current over a fixed capacitance. The balancing action is obtained by a second capacitor biased by a sine wave opposite in phase with same frequency and suitable amplitude, as Fig. 2(a) shows. If $C_sV_s = C_fV_f$, then the sine wave at the measurement frequency in the midpoint has zero amplitude. An interfering sine wave coupled to V_X through the parasitic capacitance C_p generates a sine wave at the mid point multiplied by $C_p/(C_p + C_s + C_f)$, less than one independently on the extent of the parasitic coupling. An advantage of the method is that the network is passive and no saturating condition can affect the voltage of the intermediate point.

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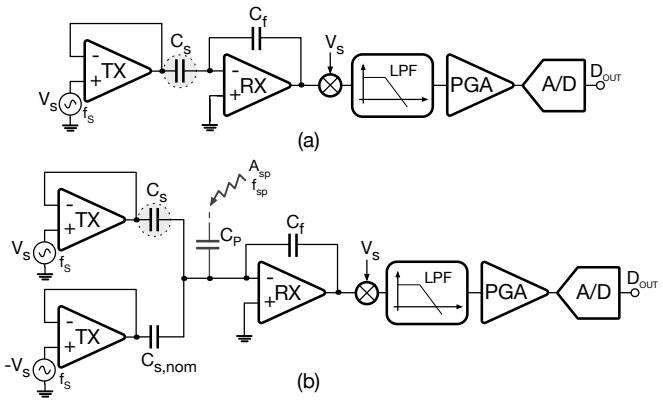

Fig. 1. (a) Conventional sensor interface. (b) Improved conventional sensor interface.

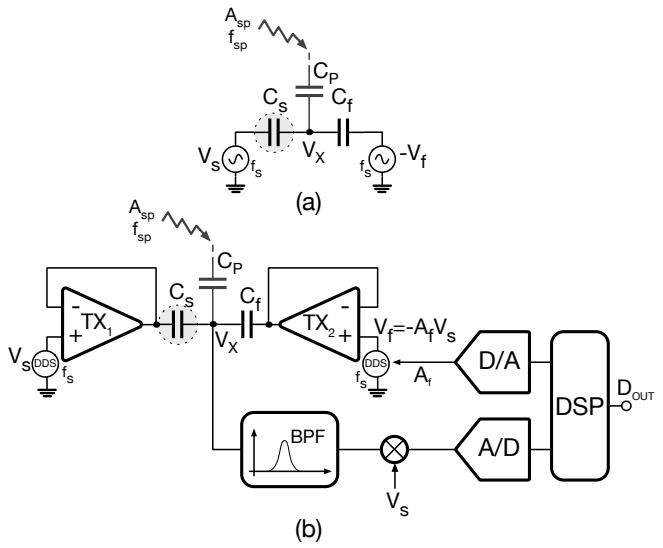

Fig. 2. This sensor interface. (a) Basic idea. (b) Architecture.

The balancing condition can be ensured by a feedback loop that controls the amplitude of the V_f generator. Fig. 2(b) shows the architecture. The first transmitter (TX_1) applies a sinusoidal signal V_s on the sensor capacitance C_s, while the second transmitter (TX_2) applies a signal opposite in phase with amplitude A_f on the feedback capacitance C_f. The amplitude of the signal transmitted by TX_1 is constant and equal to A_s, while the amplitude of the feedback signal V_f makes $V_x = 0$ V at the operating frequency. Since

$$V_x = V_f \frac{C_f}{C_s + C_f} - V_s \frac{C_s}{C_s + C_f} \tag{1}$$

the feedback loop nulls V_x with

$$V_f = V_s \frac{C_s}{C_f} \tag{2}$$

The capacitor C_p just attenuates the amplitude of V_x, thus reducing the sensitivity of the measurement but it does not affect the signal at the measurement frequency. Therefore, the system must rely on the ability of the feedback control to reject out of band spurs and to compensate for the attenuation caused by C_p.

A suitable band-pass filter rejects interferences at node V_x. It is used before the mixer that brings the signal around DC. The latter is converted in the digital domain by an ADC. The digital output is processed in order to generate the digital control of the DAC that determines the full scale amplitude of a direct digital synthesiser (DDS) sine wave generator. At every conversion cycle, the DAC output starts from a nominal fixed value or a value decided by the DSP and searches the zero condition. The DSP enables adjusting the loop gain during the acquisition cycle. At the beginning the gain is high for a fast tracking, then the gain becomes low for ensuring high-resolution and stability.

As discussed in details in the next section, the used filter is sampled data. This does not require to generate a continuous-time sine wave as it is necessary for the architecture of Fig. 1. A stepwise pseudo sine wave can be used instead. Therefore, the DDS generators are required to give rise at the output a limited number of discrete levels. This and the balanced architecture allows to match TX_1 and TX_2 and to compensate for non linearities in the buffers. Suitable number of steps for the generated signals are 8 or 16. This requires using a clock 8 or 16 times the measurement frequency.

IV. Band-Pass Filter

The availability of a clock synchronous with the samples of the stepwise sine wave can be advantageously exploited for the design of the bandpass filter. An appropriate possible solution is the N-Path scheme, [4], that uses N sections to process one sample per period of the input at the nominal bandpass frequency. As known, the N-path filter, whose architecture is shown in Fig. 3(a), implements the transformation $z \rightarrow z^N$. Therefore, if the path transfer function, $H_p(z)$, is low pass with poles at z_i, the frequency response of the N-path gives rise to N replicas of the poles z_i distributed around the unity circle. The result, as illustrated by Fig. 3(b), is that in addition to a low-pass response, multiple band-pass responses result.

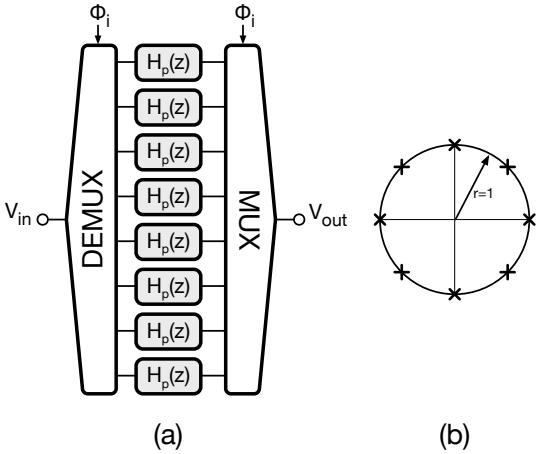

Fig. 3. N-Path filter. (a) Architecture. (b) Pole positions.

Each channel is an approximate integration with transfer function $H(z) = \beta z^{-1}/(1-\alpha z^{-1})$, where $\beta/(1-\alpha)$ is the low frequency gain. For a passive SC-C implementation its value is 1. The filter transfer function becomes

$$H(z)_{N\_PATH} = \frac{\beta z^{-N}}{1-\alpha z^{-N}} \quad (3)$$

that is like the one in Fig. 4(a) for N=8. The channels of the N-path equal the number of phases used in the DDS generation of the transmitted signal. The multiple band pass is beneficial but, if the interferer frequency is a multiple of the operating frequency, this would pass unaltered the N-Path filter. The solution to this problem is to incorporate a low-pass filter within the N-path in order to reject interferers at a frequency higher than the operating one. There is a trade off between filter efficiency and complexity. The used solution takes advantage of the already available paths in order to implement an 8-paths finite impulse response filter (FIR) that places zeros at multiples of the operating frequency. The corresponding transfer function is

$$H(z)_{FIR} = z^{-2}(1 + \frac{\sqrt{2}}{2}z^{-1} + z^{-2} - z^{-4} - \frac{\sqrt{2}}{2}z^{-5} - z^{-6}) \quad (4)$$

Two extra delays match the timing of the 8-path filter. Since the values of the coefficients must be realised with capacitance ratios it is convenient to approximate $\sqrt{2}$ to a more convenient value. Fig. 4(b) shows the magnitude plot with non unity coefficients set to 1.4. The FIR response combined with the one of the N-path gives rise to the magnitude plot of Fig. 4(c).

Having three positive coefficient and three negative coefficients in each integrator of the N-path filter allows a simple implementation combined with the single ended to differential conversion. The terms are stored in capacitors with proper weight, then the charges are injected simultaneously on the two sides of a fully differential integrator as shown in Fig. 5. The circuit uses 8 generic consecutive phases. The first one samples the input on a $2C_u$ capacitance and injects the charge after 8 delays. During the second phase a $3C_u$ capacitance samples the input and injection occurs after 7 delays and so forth. The sign of coefficients results from the injections into one of the complementary inputs. The fully differential operation rejects the common mode component of the positive and negative

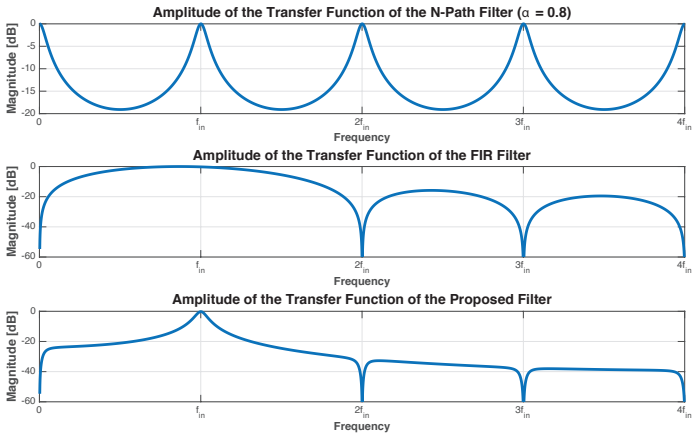

Fig. 4. Amplitude plot of the transfer functions of the combined filters. (a) N-Path filter. (b) FIR filter. (c) Proposed filter.

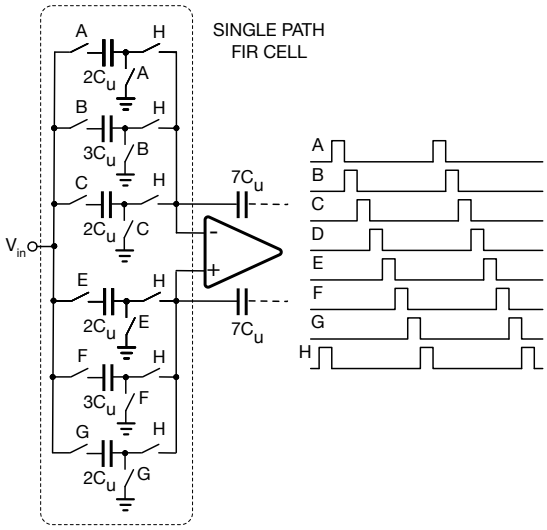

Fig. 5. Fully differential schematic of the FIR used in each path.

terms. With an integrating capacitor of $7C_u$ the differential output is amplified by 2.

After the two filters, FIR and N-path, the signal must be mixed with the transmitted stepwise sine wave. Remind that the voltages at the output of each path are samples of the signal at successive sampling times; so they must be multiplied by the weight defined by the mixing signal. For an 8-path architecture, the multiplying factors are $\sqrt{2}/2$, 1, $\sqrt{2}/2$, 0, $-\sqrt{2}/2$, -1, $-\sqrt{2}/2$, and 0. All these multiplications can be incorporated in the N-path filter as Fig. 6 shows. It is an 8 channels N-path with two paths removed because of the zero multiplying coefficients. Each path uses the FIR structure of Fig. 5. The negative sign is obtained by reversing the differential signal to send at the ADC input. The value of the integrating capacitors should match the related coefficient. Indeed, the $\sqrt{2}/2$ factor can be rounded to 0.7 and obtained simply by the use of 7 and 10 integrating unity capacitors across the op-amp serving the related path.

The signal processing provides the digital result and generates the control of the DAC used to drive the DDS that generates the stepwise sine wave V_f. The gain of the loop controlling the amplitude of V_s varies during the measurement for an optimal search algorithm.

V. Simulation Results

The proposed sensor interface has been simulated at behavioural level in the Simulink environment. Fig. 7 shows the Matlab model block diagram. An adder collects the input signals at the residue node V_X. The model allows to account for thermal noise n(t) and EM interferers. The model of the N-Path filter uses delays cells to generate the 8 paths of the signal. The addition of the paths gives rise to the input of the analog-to-digital converter. The DSP block allows pre-amplification to change dynamically the loop gain, a second order integrator and a low-pass filter. After processing, the digital signal is converted back to analog to control the full scale amplitude of V_f. The digital output of the DSP also provides the value of the measurement.

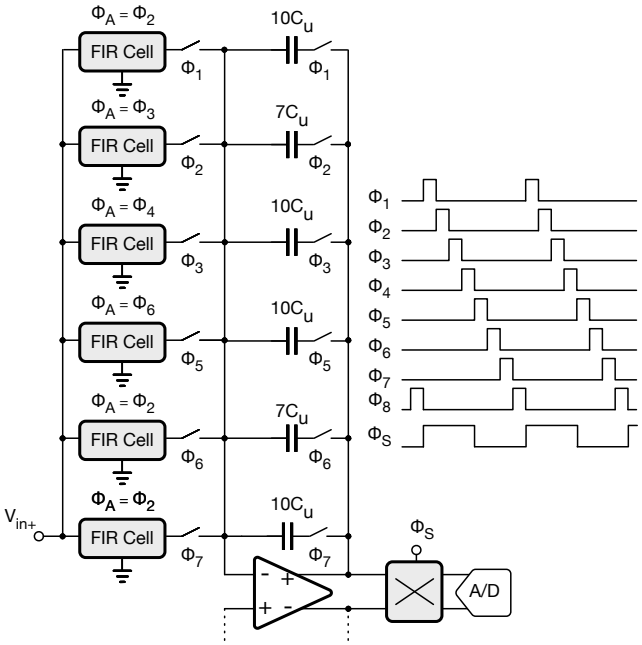

Fig. 6. Complete FIR/N-Path and mixer circuit.

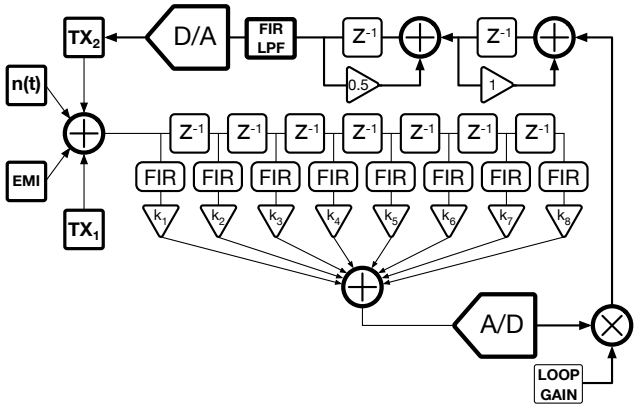

Fig. 7. Matlab model of the system used for simulations.

The pseudo sine wave frequency is $f_{TX1} = 10$ MHz, so the clock runs at 80 MHz. The accuracies of the ADC and the DAC are 10 and 12 bit respectively. The values can be scaled depending on specific system requests. The measurement starts with a setting of the DAC at zero or half of the full scale. The output of the DSP augments (or diminishes) the DAC setting until reaches the balance condition. At the beginning of the measurement the loop gain is high and after a pre-defined number of sine wave periods it is reduced for a smooth settling to the final value. Filtering the 12-bit control of the DAC improves the measurement accuracy.

Fig. 8 shows the transient response of the DAC control for $C_s = 0.8743C_F$ in the configuration that initially forces the output of the DAC to 0 V. The chosen DSP parameters allow a settling of the measurement with 1 LSB accuracy within 4 μs. The loop gain is reduced by a factor 4 after 2 μs.

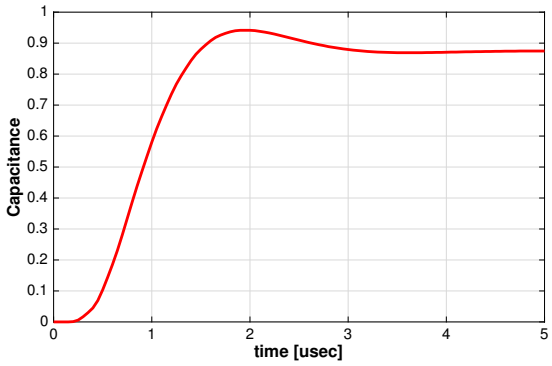

Fig. 8. Transient response of the tracked capacitance amplitude.

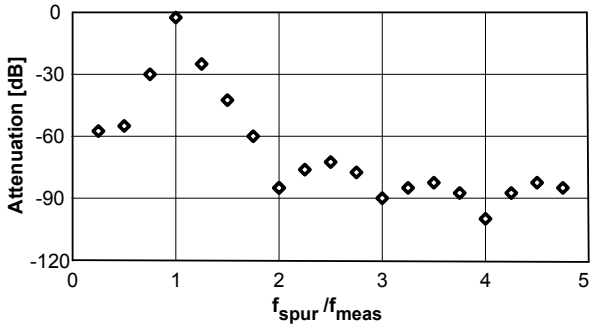

Fig. 9. Attenuation of spur versus frequency.

The rejection of spurs depends on the frequency at which the interference occurs. Obviously a spur at the same frequency of the measurement passes without attenuation. For other frequencies the rejection is the one depicted in Fig. 9. The attenuated spur for $f_{spur} \geq f_{meas}$ stays below the quantisation noise introduced by the 12-bit DAC.

VI. Conclusions

A novel feedback based interface for capacitive sensors operating in hostile environments has been presented. A particular data sampled band-pass filter allows the interface to filter out EM interferers in the band of interest. Behavioural level simulations demonstrate the effectiveness of the idea for 12-bit resolution.

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