A Mode-of-Operation Based Switching Technique for SIDO Buck-Boost Converter

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***Abstract*—This article presents a switching technique for the Single Inductor Double Output (SIDO) buck-boost converter. The proposed switching technique improves the overall efficiency of the SIDO DC-DC converter by (i) automatically differentiating between buck and boost dominated modes of operation and (ii) providing a need-based charging phase to the system only in the boost-dominated load conditions. In addition, using the proposed technique, the outputs are regulated efficiently across the input/line variations. The generation of switching phases is entirely by error processing and simplified. System level simulation of the SIDO buck-boost converter is performed and the relevant results are provided.**

I. Introduction

The modern electronic systems catering to various applications like the industrial, automotive and portable systems require multiple dc power supplies to optimize the system performance metrics. Some of these applications also require integrated circuits functional in the presence of widely fluctuating battery supplies. The power-management experts often trade among the design parameters viz. efficiency, noise immunity and silicon integrability in the generation of regulated supplies. Owing to their superior efficiency, the switched DC-DC converters are often favored over the linear regulators. In the aforementioned, multi-supply requiring applications, the minimization of PCB area and BoM underscores the suitability of Single Inductor Multiple Output (SIMO) DC-DC converters.

Over the years, several articles have reported the implementation of SIMO/SIDO DC-DC converters [1]–[10]. The ease of implementation, improvement of cross/line/load regulation, and higher efficiency have been the design goals of the reported SIMO DC-DC converters. Of particular interest, among the SIMO converters, are the ones that provide buck-boost regulated voltages. The buck-boost feature of the SIMO/SIDO may be needed to address the buck and boost nature of the required load voltages and/or the battery dynamics. A SIDO buck-boost converter implemented in [4] uses adaptive current control mode (ACCM) to reduce cross-regulation and power losses. A SIMO auto buck-boost converter implemented in [5] solves the problem of unbalanced loading of different channels and attains higher efficiency by using the technique of auto-phase allocation and a 1st order PLL. In [6], a SIDO buck-boost converter is proposed with an extended-PWM control to select buck and/or boost modes and maintain high efficiency. Similarly in [7], a SIDO step-up/down converter is simulated with integrated charge control in pseudo-continuous conduction mode (PCCM) to minimize cross regulation. Another SIMO buck-boost converter reported in [8] uses tail current control and frequency control loop to achieve robust reference tracking and higher power efficiency. In general, the previously reported articles on SIMO/SIDO buck-boost DC-DC converters mainly address cross regulation and power efficiency. The average inductor current and the efficiency are a strong function of the switching period and the order of switching. A simplified control strategy that controls the switches adaptively depending on the load and line conditions can greatly improve the efficiency.

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In this paper, the SIDO buck-boost converter with the proposed error based controller effectively senses the buck/boost dominated load and line conditions and accordingly adapts the switching order to enhance the efficiency. The proposed technique is particularly marked by the simplicity as detailed in the following Sections.

II. SIDO Buck-Boost Converter: Review

A SIDO buck-boost converter power stage and all the possible sequential turn-on paths *[A-F]* at different instances in a switching period of the converter are shown in Fig. 1(a) and Fig. 1(b). The path *[C]* charges the converter, *[A]* and *[D]* constitute the bypassing phase, *[B]* and *[E]* discharge the converter and the path *[F]* is the freewheeling path. The choice of the sequence/order of converter charging, bypassing and discharging phases determines the sequence of turn-on paths in a switching period.

Before the proposed converter switching sequence is introduced, the power stages of the SIDO/SIMO converters in the state-of-the-art articles may be discussed. Traditionally, time multiplexed continuous conduction mode (CCM) SIDO buck-boost converters follow the switching sequence *[A-B-C-D]*. A freewheeling path *[F]* is used to achieve PCCM mode, [9]. However, the reduction in the number of switchings per cycle offered by ordered power distributive control has resulted in its wider acceptability, [5]. In [6], the CCM SIDO converter uses the sequence *[C-A-D-E]* in the buck-boost mode. The charging phase *[C]* is chosen by default at the beginning of each cycle. Similarly in [4], the sequence *[C-A/D-B/E-F]* is used for each output of the SIDO. The SIMO converter in [10] although uses two different modes viz. PWM and hysteresis modes to control the power stage, both the modes require the charging phase. The step-up/down SIDO in [7] relies entirely on the charging path *[C]* to energize the converter.

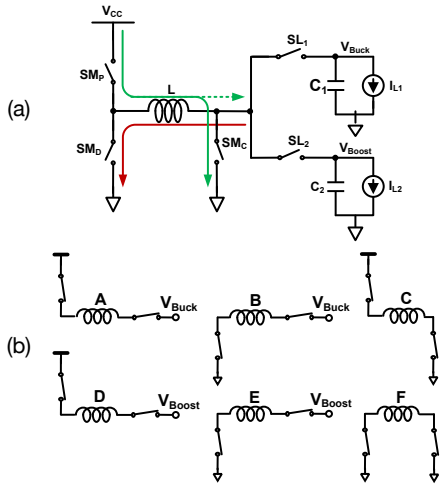

Fig. 1. (a) SIDO buck-boost converter power stage. (b) Possible turn-on phases in the converter.

The charging phase *[C]* in the SIDO/SIMO converter leads to increased average inductor current. However, the loads are not charged during this phase. As a result, the average inductor current exceeds the total average current delivered to the loads. This increment in the average current of the inductor leads to loss of efficiency in the converters. Hence, to minimize or alleviate the charging phase *[C]* is an objective in the design of efficient SIDO/SIMO buck-boost converters. The buck and boost loads can be relatively tracked and the co-occurrence of charging phase *[C]* and bypassing phase *[A]* in a single switching period may be minimized under some of the loading conditions. This observation is made by some of the recent articles [5], [8]. However, the control method adopted in [5] and [8] to generate the load dependent phases *[A-F]* is quite complex. A relatively simpler and effective phase generation and switching method for a SIDO buck-boost converter is proposed in the following Section. This technique tracks both the relative load conditions of the sub-converters and the input/line variations to generate a need-based charging phase *[C]* and improve the efficiency of the converter.

III. Proposed Efficient Switching Technique for SIDO Buck-Boost Converter

In the CCM SIDO buck-boost converters, the load requirement of each sub-converter decides its energizing phase fed by the inductor. A buck-boost converter may be differentiated into buck dominated and boost dominated modes of operation. In a buck-dominated mode the power delivered to the buck sub-converter well exceeds the power delivered to the boost sub-converter. In the boost-dominated mode, the power delivered to the boost sub-converter is higher. In the proposed SIDO buck-boost converter, with the power stage as shown in Fig. 1(a), the buck dominated mode is favourably used to alleviate the charging phase *[C]* to improve the efficiency of the converter. In the boost dominated and balanced modes (similar buck and boost load current requirement) the charging phase *[C]* is introduced to regulate the outputs.

Fig. 2 shows the system level of the proposed SIDO buck-boost converter. The system is controlled entirely by error

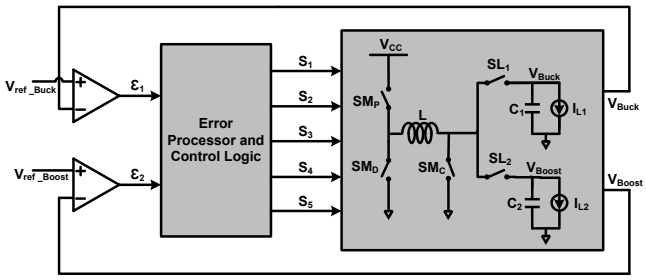

Fig. 2. System level block diagram of the proposed CCM SIDO buck-boost converter.

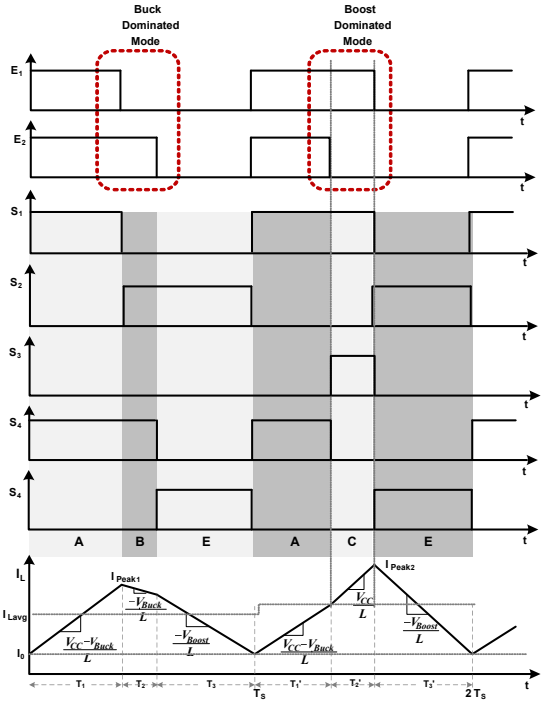

Fig. 3. Timing diagram of the proposed SIDO buck-boost converter.

processing. The error processor tracks the mode of operation of the converter as well as the input/line variations. The errors ε_1 and ε_2 are processed to generate the control signals S_1-S_5. The signals S_1, S_2, S_3, S_4, and S_5 drive the switches SM_P, SM_D, SM_C, SL_1, SL_2 respectively in the power stage.

A. Error processing and generation of driving signals

The errors ε_1 and ε_2, generated by comparing the two regulated outputs with the corresponding references, are summed and differenced to obtain $(\varepsilon_1+\varepsilon_2)$ and $(\varepsilon_1-\varepsilon_2)$. $(\varepsilon_1+\varepsilon_2)$ and $(\varepsilon_1-\varepsilon_2)$ are further processed and Pulse Width Modulated (PWM) to E_1 and E_2 shown in Fig. 3.

The signal E_1 represents the total system error and the signal E_2 relatively compares the sub-converter errors. The power stage driving signals S_1-S_6 are digitally derived from E_1 and E_2. Fig. 3 shows the two modes of functioning of the SIDO converter. In the buck dominated mode, the inductor is sufficiently charged while feeding the buck stage and supplies the boost sub-converter without requiring additional charging phase *[C]* and its driving signal S_3. However, in the boost

dominated mode, the buck sub-converter insufficiently charges the inductor. The charging phase *[C]* is derived to extra-charge the inductor to feed the boost sub-converter. The novelty of this work is the need-based generation of charging phase *[C]* to improve the overall efficiency of the SIDO converter.

The buck or boost dominated modes are a function of the load currents and input (line). This is critical if the regulated output (buck/boost) voltage is not fixed but linear function of the input/line. The proposed error based switching signal generation technique tracks both the load and line variations and maintains the minimum average inductor current I_{Lavg}. As conceptually evident in Fig. 3, I_{Lavg} and I_{Peak} vary with the mode of operation of the SIDO converter.

B. Analysis: proof of concept

In the buck-dominated mode of operation of the SIDO buck-boost converter, the average inductor current I_{Lavg} in Fig. 3 may be written as in (1)

$$I_{Lavg} = I_0 + [\alpha D_1 + \beta D_2 + \gamma D_3]/2L \tag{1}$$

where $\alpha = (V_{CC} - V_{Buck})(T_1 + T_2)$, $\beta = -V_{Buck}T_2$, $\gamma = V_{Boost}T_3$, and $D_i = T_i / T_S$ corresponds to the duty cycle of each phase T_i .The inductor supplies load current in all the three phases. Similarly the average inductor current in the boost-dominated mode is given by (2)

$$\begin{aligned} I_{Lavg} \quad = \quad & \left[\left(\frac{T_1'}{2L}(V_{CC} - V_{Buck}) + I_0\right)D_1' + \left(\frac{T_3'}{2L}V_{Boost} + I_0\right)D_3'\right] + \\ & \left[\left(\frac{T_1'}{L}(V_{CC} - V_{Buck}) + \frac{T_2'}{2L}V_{CC} + I_0\right)D_2'\right] \end{aligned} \tag{2}$$

Equation (2) consists of two components in the squared brackets. The first component is the inductor current delivered to the loads and the second term corresponds to the inductor ground-charging current. Clearly, the inductor ground-charging current is determined by the inductor grounding signal S_3 (with duty cycle D_2'). Hence, it is the objective of the proposed SIDO converter and the switching technique to generate need-based S_3 depending on the load/line conditions.

In the presence of large variations in the input (line) voltage, the converter is required to regulate the outputs over the entire range of line variations. Without the inductor grounding phase *[C]*, the SIDO regulation is limited to a minimum value of V_{CC} (V_{CCMin}) for each load condition. As shown in (3), V_{CCMin} is a strong function of the load currents (thereby corresponding duty cycles D_{Buck} and D_{Boost}).

$$V_{CCMin} = D_{Buck}V_{Buck} + D_{Boost}V_{Boost} \tag{3}$$

Using the grounding phase *[C]* with duty cycle D_{Gnd}, this limitation is overcome in the SIDO/SIMO buck-boost converters. The phase *[C]* adds extra degree of freedom in (3) to reduce the minimum supply V_{CCMin} required to achieve regulation. As shown in (4) and (5), V_{CCMin} may reach the limiting minima up to V_{Buck} to sustain buck-boost regulation. Equation (4) corresponds to the inductor charge-discharge cycle *[A-C-D]* whereas (5) corresponds to the cycle *[A-C-E]*

TABLE I. System specifications.

V_{CC}	10/15 V
Switching frequency	2 MHz
V_{Buck}, IL_{Buck}	5 V, 20 mA−100 mA
V_{Boost}, IL_{Boost}	V_{CC}+5 V, 20 mA−100 mA

which is used in the proposed switching technique. In (4) and (5), $D_{Buck}+D_{Boost}+D_{Gnd} = 1$.

$$V_{CCMin} = \frac{D_{Buck}V_{Buck} + D_{Boost}V_{Boost}}{D_{Buck} + D_{Boost} + D_{Gnd}} \tag{4}$$

$$V_{CCMin} = \frac{D_{Buck}V_{Buck} + D_{Boost}V_{Boost}}{D_{Buck} + D_{Boost}} \tag{5}$$

IV. System Simulation Results

The proposed SIDO buck-boost converter is modelled and simulated at the behavioral level. The system level specifications used in the simulation are tabulated in Table I. The specifications resemble the requirements in automotive and industrial applications. The buck and boost load currents (IL_{Buck}, IL_{Boost}) vary randomly in the range 20 mA−100 mA. As a result, the mode of operation of SIDO converter varies between buck and boost dominated modes.

The other important simulation parameters used are as follows: L=10 µH, C_1= C_2=10 µF, R_{ESR_L}=200 mΩ, R_{Switch}= 2 Ω. Fig. 4(a) and Fig. 4(b) show the control signals and the regulated outputs of the proposed SIDO buck-boost converter as the load currents vary.

The results in Fig. 4 and Fig. 5 are obtained using Matlab-Simulink based model of the system. The signal

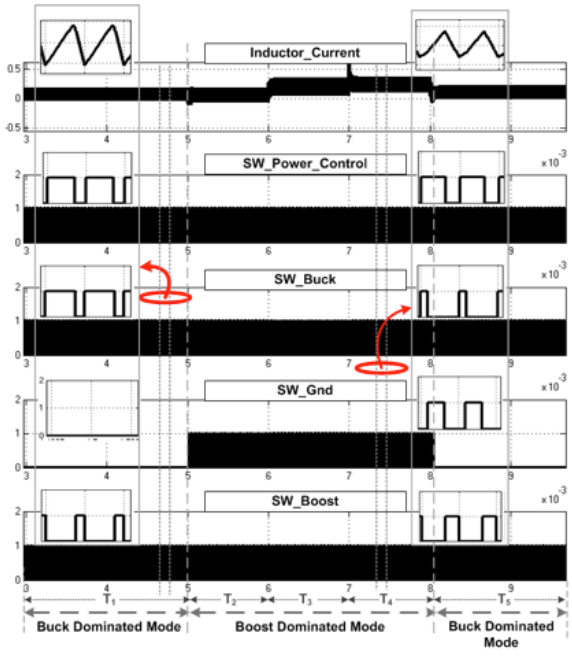

Fig. 4. Control Signals of the SIDO converter.

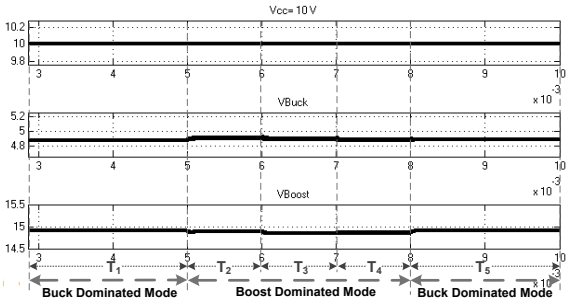

Fig. 5. Regulated outputs of the SIDO converter: V_{Buck}=5V and V_{Boost}= V_{CC}+5 V.

SW_Power_Control in Fig. 4 controls the complementary switches SM_P and SM_D in the power stage in Fig. 1(a).

In Fig. 1 and Fig. 5, the variations in load currents, IL_{Buck} and IL_{Boost}, of the two regulated outputs modify the mode of operation of the converter. During T_1, IL_{Buck}=80 mA and IL_{Boost}=20 mA which corresponds to the buck dominated mode and the signal *SW_Gnd* that controls the grounding phase *[C]* is disabled. The converter follows the switching sequence *[A-B-E]*. During T_2+T_3+T_4, the converter enters the boost dominated mode. The load conditions during boost dominated mode are as follows – T_2: [IL_{Buck}= 20 mA, IL_{Boost}=20 mA], T_3: [IL_{Buck}= 20 mA, IL_{Boost}=80 mA], T_4: [IL_{Buck}= 100 mA, IL_{Boost}=80 mA]. During T_5, the converter returns to buck dominated mode with IL_{Buck}= 100 mA and IL_{Boost}=30 mA. As evident in Fig. 5, the outputs are regulated across the modes of operation of the converter. A maximum ripple voltage of 60 mV is observed.

In some of the industrial/automotive applications, a step up mode of operation is required to enhance the performance of the system. The input supply is stepped up to achieve improved performance. The proposed converter tracks such step-up/down operations and regulates the outputs accordingly. As shown in Fig. 6, during step-up/down V_{Buck} is a regulated at 5 V and V_{Boost} (=V_{CC}+5 V) linearly tracks V_{CC}. In the transient shown, the converter is boost-dominated during step-up and buck-dominated during step-down.

In order to emphasize the contribution of on-demand ground-charging of the inductor in improving the efficiency of the converter, a simulation was carried out with/without inductor ground-charging in a buck-dominated load condition. In the buck-dominated mode, the converter does not require the ground-charging phase. Following the conventional method, if a non-essential inductor grounding phase *[C]* is introduced, a degradation of the efficiency is observed. Fig. 7 shows this

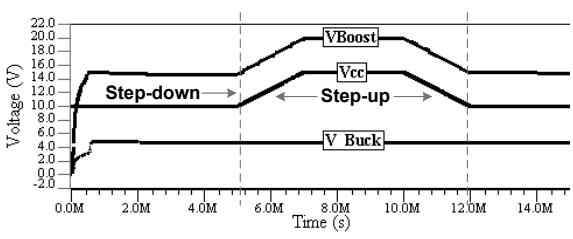

Fig. 6. SIDO converter response during V_{CC} step-up and step-down.

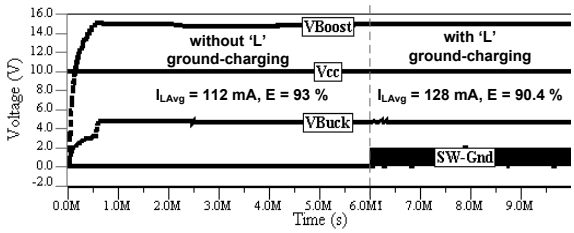

Fig. 7. Comparison of efficiency (E) in a buck-dominated mode with/without L ground-charging phase *[C]*.

comparison. The proposed technique improves the efficiency (E) by 3%. The results in Fig. 6 and Fig. 7 are obtained using the Spice-VerilogA behavioral model of the system.

V. Conclusion

A SIDO buck-boost converter with a novel switching technique in the power stage is introduced. The converter automatically differentiates between buck and boost dominated modes of operation. The corresponding, on-demand extra-energizing of the system significantly enhances the converter efficiency. The error-processor based control signal generation is simplified in comparison with the earlier works. Brief analysis and behavioral level simulations are reported to demonstrate the advantages of the proposed architecture.

References

[1] D. Kwon and G.A. Rincon Mora, "Single-inductor-multiple-output switching DC-DC converters", *IEEE Transactions on Circuits and Systems - II*, vol. 56, no. 8, pp. 614-618, 2009.

[2] M. Belloni et al., "A 4-output single inductor DC-DC buck converter with self-boosted switch drivers and 1.2 A total output current", *IEEE International Solid State Circuits Conference (ISSCC) Dig. Tech. Pap.*, pp. 444-445, Feb. 2008.

[3] M.-Y. Jung et al., "An error-based controlled single-inductor 10-output DC-DC buck converter with high efficiency at light load using adaptive pulse modulation", *IEEE International Solid State Circuits Conference (ISSCC) Dig. Tech. Pap.*, pp. 222-223, Feb. 2015.

[4] M.-H. Huang and K.-H. Chen, "Single-inductor dual buck-boost output (SIDBBO) converter with adaptive current control mode (ACCM) and adaptive body switch (ABS) for compact size and long battery life in portable devices", *IEEE Symposium on VLSI Circuits Dig. Tech. Pap.*, pp. 164-165, 2009.

[5] Y. Zheng et al., "A single-inductor multiple-output auto-buck-boost DC-DC converter with autophase allocation", *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2296-2313, 2016.

[6] W. Xu et al., "A 90% peak efficiency single-inductor dual-output buck-boost converter with extended-PWM control", *IEEE International Solid State Circuits Conference (ISSCC) Dig. Tech. Pap.*, pp. 394-395, Feb. 2011.

[7] S.-C. Koon, Y.-H. Lam, and W.-H. Ki, "Integrated charge-control single-inductor dual-output step-up/step-down converter", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3071-3074, May 2005.

[8] Y. Zheng et al., "A single-inductor multiple-output auto-buck-boost dc-dc converter with tail-current control", *IEEE Transactions on Power Electronics*, DOI: 10.1109/TPEL.2015.2512619.

[9] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching", *IEEE Journal of Solid State Circuits*, vol. 38, no. 1, pp. 1007-1014, June 2003.

[10] M.-H. Huang and K.-H. Chen, "Single-inductor multi-output (SIMO) DC-DC converters with high ligh-load efficiency and minimized cross-regulation for portable devices", *IEEE Journal of Solid State Circuits*, vol. 44, no. 4, pp. 1099-1111, Apr. 2009.