Multichannel Time Interleaved ADC for Sensor Interfaces

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***Abstract*—A possible architecture of time-interleaved Incremental extended-range ADC (TIADC) is presented. In this paper, the operation of proposed TIADC including a SAR as extended range A/D is described. The limits finite op-amp gain and mismatch between the time-interleaved channels is analyzed. A solution that limits the effect of mismatch to small gain errors in each channel is discussed. Simulation results provide design direction for obtaining high-resolutions ADC converters. The use of op-amp with more than 90 dB gain allows achieving resolutions in the 14 bit range or more.**

I. Introduction

As Internet of Everything (IOE) evolves, more integrated sensor interfaces have been required. Typical sensor application include image sensors, weight scales, digital voltmeters, as well as temperature, magnetic, pressure for wearable devices. Analog-to-digital converter (ADC) is a critical part of integrated sensor on a system-on-chip (SoC).

Delta-Sigma ($\Sigma\Delta$) modulation is a relatively simple means of performing high-resolution data conversion. A major shortcoming of ($\Sigma\Delta$) modulators, however, is the limitation in their application to relatively narrow bandwidth signals due to the oversampling requirement. Incremental ADCs are Nyquist-rate ADCs which use oversampling and noise shaping to convert a finite number of analog samples into a single digital word. In fact, they are a hybrid of Nyquist-rate and ($\Sigma\Delta$) ADCs with exception that integrators are reset after each conversion. Internally the incremental ADCs are operating at higher sampling rate [1], [2]. Incremental ADCs can be time-interleaved by placing N incremental ADCs in parallel, which results in an effective sampling frequency of $N.f_s$ as well as, for an oversampling rate (OSR) of M, this can be viewed as effectively reducing the OSR to M/N, resulting in an increase in the signal bandwidth by N. It is easy to combine a TIADC with a Nyquist-rate ADC to perform extended range conversion and achieve the advantages of both oversampled and Nyquits-rate ADC as well as high resolution with maximum energy efficiency [3], [4].

Fig.1 shows the proposed time-interleaved incremental ADC with an extended A/D converter operating at Nyquist-rate, it consists of N channels. The extended A/D could sample the residue voltage right before the reset pulse, and performs the fine quantization. The overall performance of time-interleaved incremental ADC is sensitive to channel mismatch [5].

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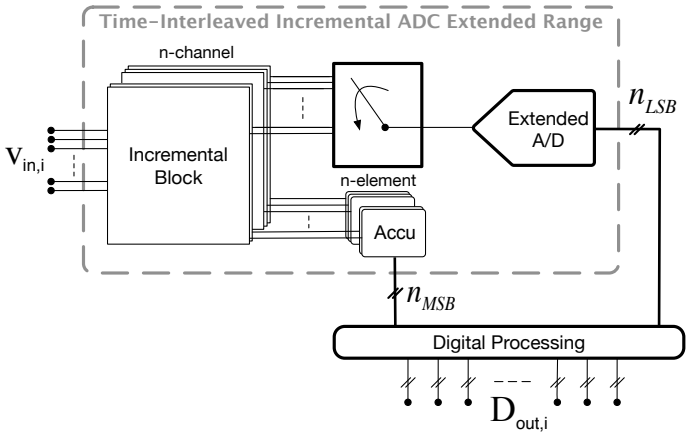

Fig. 1. Proposed system level diagram of multichannel time-interleaved incremental ADC (TIADC) with extended range A/D.

This paper will discuss a proposed architecture for time-interleaved incremental ADC, included the possible circuit implementation and studies the limits caused by offset and gain channel mismatch. Section II introduces architectures of a TIADC for sensor applications. Section III propose solutions regard channel mismatch in the proposed TIADC. Section IV briefly discusses the limitation caused by non-idealities of the op-amp and DAC in incremental data converter as well as time-interleaved ($\Sigma\Delta$) modulators, and section V concludes the paper.

II. Time Interleaved Incremental ($\Sigma\Delta$) ADCs

Fig. 1 shows the concept on which this time-interleaved converter is based. The multiple inputs (Vin, i) drive n-channels of a time-interleaved first order modulator. The outputs are an interleaved bit-stream and the voltage across the op-amp used in the incremental scheme. Accumulators process the digital outputs to generate the MSBs. At the end of the incremental conversion the residual, stored on capacitors is sequentially converted by a SAR to obtain the bits that extend the range of the conversions.

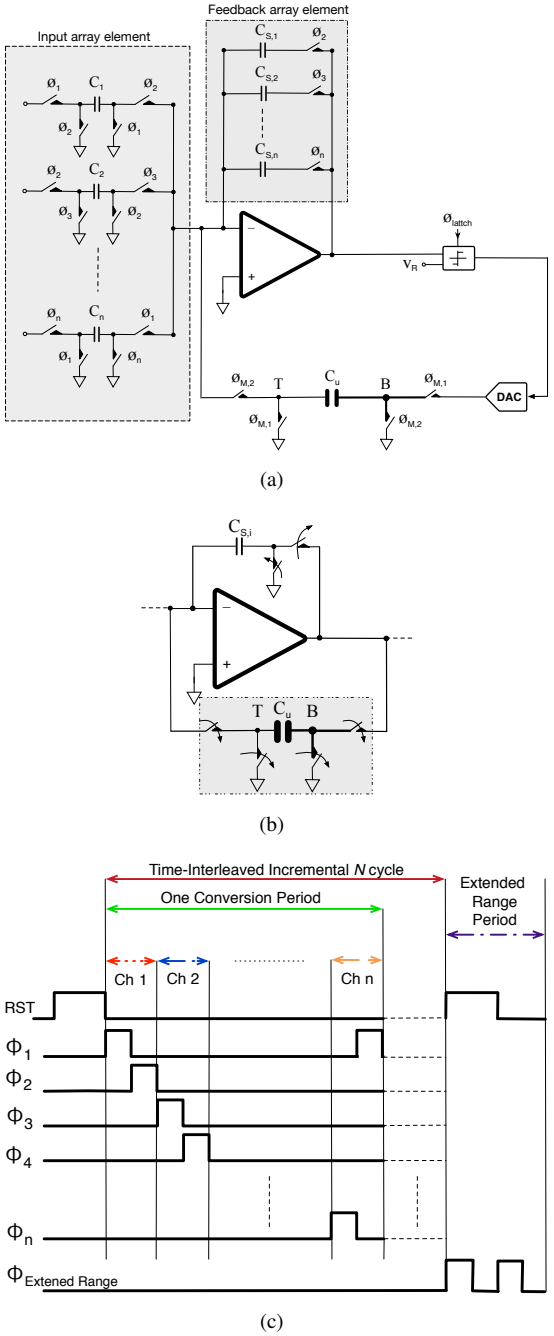

Fig. 2. (a) Proposed circuit architecture for TIADC. (b) Charge distribution reconfiguration. (c) Simplified timing diagram for proposed TIADC with extended range A/D.

As known time-interleaved incremental ADC uses a global reset to clear the memory and to output the data functioning as a Nyquist-rate ADC [3]. A Nyqusit-rate solution is more suitable for use in a sensor interface than a conventional (ΣΔ) ADC for high-resolution energy-efficient data conversion. The sensor interfaces could take advantage of this technique as the area can be reduced, and the sensor made cost effective.

Fig.2(a) shows the proposed circuit architecture at the

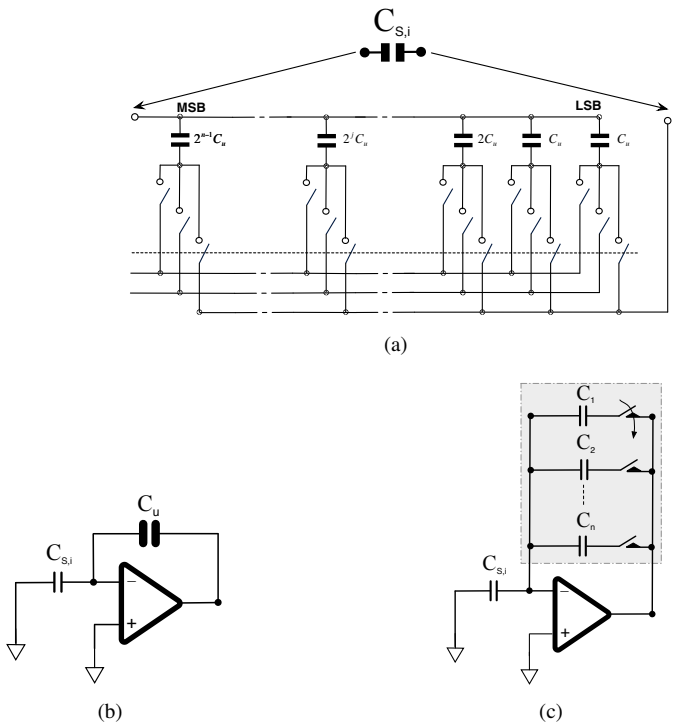

Fig. 3. Proposed channel mismatch cancellation and charge distribution solution for TIADC. (a) Use of SAR array in $C_{S,i}$. (b) Charge transfer on C_u. (c) Charge transfer on C_i.

schematic level; the simplified timing diagram of proposed TIADC, is shown in Fig.2(c). The used phases allow the sampling of the inputs sequentially; the charges sampled on capacitors C_1, ..., C_n are accumulated onto capacitors connected in feedback in a time-interleaved fashion. A single capacitor C_u performs the function required by the incremental operation. Since the input is accumulated N times while the kT/C noise is quadratically accumulated N times, that relaxed the kT/C noise requirement by $\sqrt{N}$.

The time-interleaved incremental cycle repeats for a given number of times to be followed by extended range conversions over suitably processed residual charges.

The capacitor C_u is actually a binary array of small unity elements and that array is used as basic block of a SAR converter as necessary for the extended range period. Thus a hardware-sharing has been performed to improve the energy efficiency [6]. Before the SAR conversion putting, the array preliminary discharged in feedback with the storing element grounded transfers the charge of the storing capacitors $C_{s,i}$ on it, as shown in Fig. 2(b). After the charge distribution, the capacitor C_u stores the residual and the circuit is reconfigured to determine the LSBs. Therefore C_u roles as an equivalent capacitance during the incremental and charge distribution phases and as a capacitive array for SAR operation phase.

The SAR cycle repeats for all the channels of the time-interleaved architecture.

III. Mismatch Cancellation and Charge Distribution

The mismatches between capacitors used, give rise to errors. The charge injected by each channel is proportional to the sampling capacitor. This charge is partially compensated by the one injected by the feedback element C_u. Supposing that for a given input voltage $V_{in,i}$, the comparator generates k_i ones, after N injections, at the end of the incremental phase we have

$$Q_{Cs,i} = NV_{in,i}C_i - kV_{ref}C_u \tag{1}$$

This charge gives rise to a residual voltage equal to

$$V_{out,i} = \frac{Q_{Cs,i}}{C_{s,i}} = NV_{in,i}\frac{C_i}{C_{s,i}} - kV_{ref}\frac{C_u}{C_{s,i}}. \tag{2}$$

The residual is then converted into digital to determine the LSB part of the digital code using the extended resolution approach. The number of bits of the incremental section is $n_{MSB} = log_2 N$, supposing that the fine converter determines n_{LSB} bits using V_{ref} as reference voltage, the expected overall resolution is $n_{MSB} + n_{LSB}$. However the error shown in (2) has been affected the result.

Supposing to use the SAR algorithm to generate the LSBs, it is necessary to transform the residual voltage into charge. For this we have those different options, as shown in Fig .3.

(a) Use the capacitors $C_{s,i}$ as SAR array.
(b) Transfer the charge stored on capacitors $C_{s,i}$ onto capacitor C_u.
(c) Transfer the charge stored on capacitors $C_{s,i}$ onto capacitors C_i.

The first solution is not good because the distribution determined by the SAR cycle will give rise at the input of the comparator to

$$V_{comp} = \left(NV_{in,i}\frac{C_i}{C_{S,i}} - kV_{\mathrm{Re}f}\frac{C_u}{C_{s,i}}\right) - \alpha V_{\mathrm{Re}f} \tag{3}$$

where α is the fractional part given by the SAR logic control.

The second solution obtains

$$V_{comp} = \left(NV_{in,i}\frac{C_i}{C_u} - kV_{\mathrm{Re}f}\right) - \alpha V_{\mathrm{Re}f} \tag{4}$$

while the third solution leads to

$$V_{comp} = \left(NV_{in,i} - kV_{\mathrm{Re}f}\frac{C_u}{C_i}\right) - \alpha V_{\mathrm{Re}f}. \tag{5}$$

It is evident that the both errors have affected the solution (a), while only one error has limited the two other solutions.

However, solution (c) refers to two different reference voltages ($V_{\mathrm{Re}f}\frac{C_u}{C_i}$ and $V_{\mathrm{Re}f}$) for the MSB and the LSB determination. The optimal solution is (b) which has used the same references for both conversions.

A gain error $\frac{C_i}{C_{S,i}}$ affects the result but this could possibly be corrected with digital calibration.

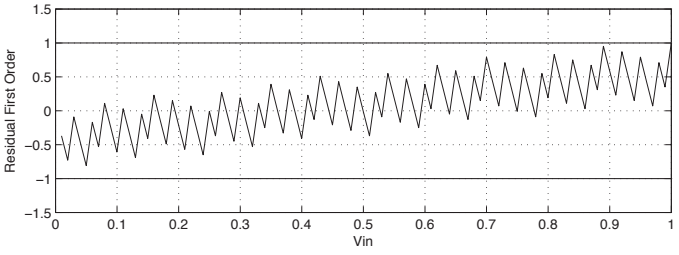

Fig. 4. Range of the residual for a single channel first order of time-interleaved incremental as function of the input amplitude.

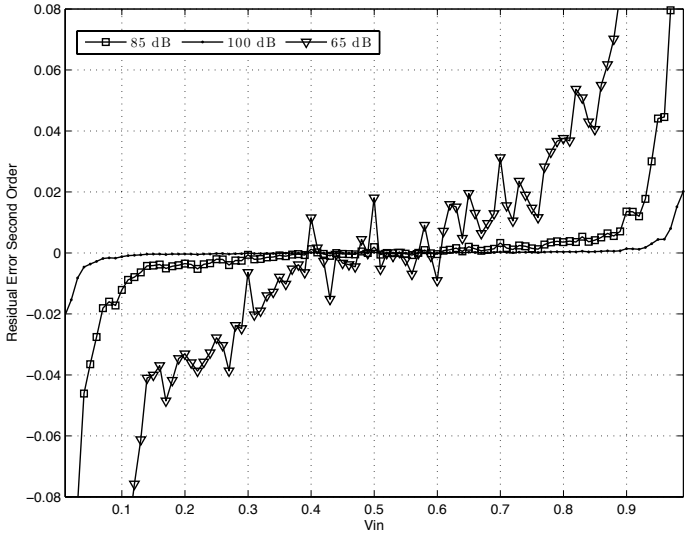

Fig. 5. Residual error of a first order converter as a function of the input amplitude for different op-amp gains.

IV. Non ideality effects and Extended Range

The limits caused by the non idealities of the op-amp such as finite gain, offset and slew rate [7] has been estimated by computer simulations. This limits the resolution added by the extended range ADC. Therefore, for a given finite gain of the op-amp it is possible to define the maximum achievable resolution and its split between the time-interleaved incremental ADC and the extended range ADC.

The value of the residual voltage depends on the input signal. Fig. 4 shows its plot for a single channel first order of time-interleaved incremental ADC modulator which has been proposed in Fig. 2(a). The error for the op-amp $gain = 80\,dB$ is within $+/-1$ LSB at 12 bit for normalized V_{in} in the $[0.1-0.9]$ range. Signals close to the boundary of the quantization interval cause distortion. In any cases, as shown, the use of single-bit quantizers make large the voltage range at input of the extended ADC. The resulting residual range which is within ± 1 means a loss of one bit in the overall resolution and the possible need an attenuation by $1/2$ at input of the extended stage.

Behavioral simulations of the first order converter with op-amp gain equal to $65\,dB$, $85\,dB$ and $100\,dB$ obtain the errors

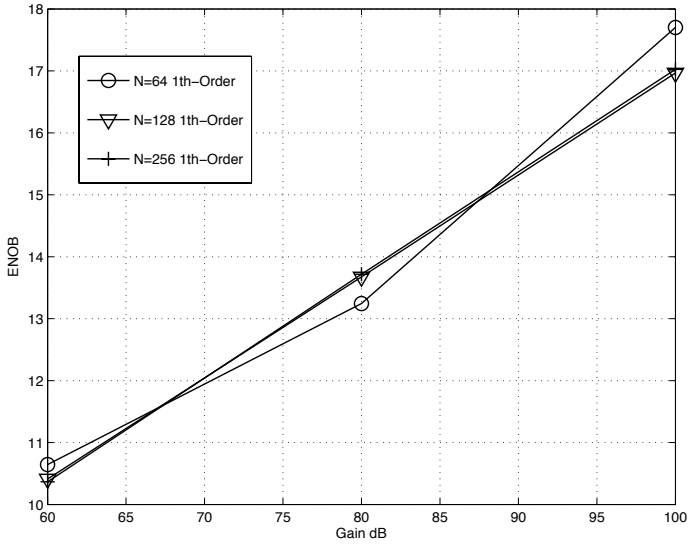

Fig. 6. Maximum achievable ENOB with an extended range incremental converter for a given op-amp DC gain.

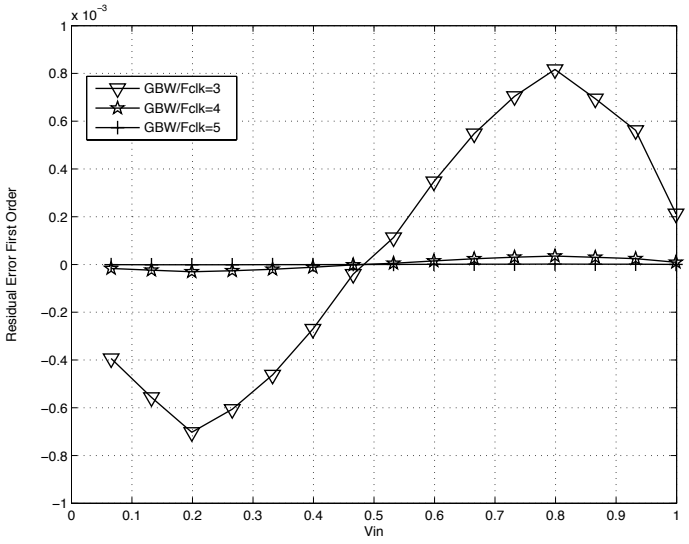

Fig. 7. Residual errors caused by slew-rate and bandwidth for the first order scheme.

of the residual signal. For a single channel first order of time-interleaved incremental converter with 64 clock cycles the errors normalized to the full scale are shown in Fig. 5. These errors are zero for a given input value and change almost linearly. The maximum variation of the error establishes the number of bits that the extended range ADC can provide (ENOB). Fig. 6 has shown the simulation result for a given op-amp DC gain equal to $90\,dB$.

Incremental converters that run for a larger number of clock periods augments the resolution: the number of levels of conversion increases linearly with N; however, the resolution error increases and the admitted resolution of the extended ADC diminishes. The result is that the total resolution is almost unchanged for larger values of N, as Fig. 6 shows.

A further limit to the resolution comes from the bandwidth and the slew-rate of the op-amp. The effect of those two parameters is non-linear and can be studied only with computer simulations. A simple approach uses the behavioral model discussed in [7]. Its use leads to the results of Fig. 7 for a first order scheme. The error with the combination of GBW and slew-rate shown in the legend is symmetrical with respect to the mid point. The figure outlines that it is necessary ensuring a GBW at least 3 times the sampling frequency to limit the error lower below the one caused by an op-amp with $90\,dB$ gain (first order scheme case). The requests are not so difficult to satisfy when using a mature integrated circuit technology. On the contrary, with nm CMOS technologies obtaining high dc gain is not easy. High bandwidth is granted without difficulty even with a relatively low consumed power.

V. Conclusion

In this paper an effective architecture for time-interleaved incremental ADC is presented. The N-times accumulation of each input reduces by $\sqrt{N}$ the value of capacitance requested by the kT/C limit. A suitable trade-off between the choice of the MSBs and the LSBs optimizes the trade-off consumed area speed of operation.

The possible limits caused by mismatch and finite gain of the op-amp have been studied. The result shows that the architecture can be a good solution for a wide range of sensor interfaces applications.

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