A Pipeline ADC for Very High Conversion Rates

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***Abstract*—This paper presents a novel pipeline configuration for wireless applications. Redundancy and multi sampling of the input techniques are used for overcoming the main limitations of pipeline ADCs. A special pre-amplifier with built-in thresholds generation is also discussed. The circuit, designed and simulated in a 65-nm CMOS technology, achieves 2.66 GS/s and 8-bit resolution. The supply voltage is 1V and the simulated power consumption is 22.06 mW, which leads to a FoM of 32.4 fJ/conversion-step.**

I. Introduction

Wireless applications require high-speed data converters operating at many GS/s conversion rate and with resolution of 8-10 bits. SAR ADCs cannot run at this very high conversion speed because the internal clock must be about ten times the sampling-rate for such a resolution. Even with nanometer technologies, it is unfeasible running SAR architectures at tens of GS/s. Moreover, power consumption increases sharply over few GS/s. The conventionally used solution to push forward the sampling-rate limits is the time interleave of ADCs: the bandwidth of an N-channel time interleaved structure is N-times the one of the single channel. The single channel architecture is often a SAR because of its simple structure that allows relatively high-speed conversion rate and low power consumption. Such an approach is limited by the fact that integrating a large number of channels complicates the clock distribution and generates sampling errors. The main issue in a time interleaved system comes from the skew from channel to channel in the sampling path. This consists in a non-periodic input sampling that reduces the maximum achievable signal-to-noise ratio and generates harmonic distortion.

Pipeline ADCs are convenient alternatives to time-interleaving. Since the stage of the pipeline is simpler than a full converter, the silicon area and consumed power are competitive. However, the problem for very high-speed pipelined architectures is the active generation of the residual, as the bandwidth of the necessary amplifiers is limited. Passive residue transfer techniques [1] can overcome this issue, but the advantage of the interstage gain that relaxes the accuracy of successive stages is lost. In addition, the speed of residual transfer cannot go up to few GHz. Other techniques, like the zero-crossing [2], pulse bucket brigade [3], and ring amplifiers [4], are power efficient alternatives to op-amps in generating residue, yet achievable bandwidth is again limited.

This paper describes a three stages pipeline with multiple sampler of input for a direct generation of residuals. The use of redundancy in the first two stages allows relaxing the comparators accuracy requirements, thus limiting the need of calibration only to the third stage. Simulation results at the post layout transistor level show that the maximum operational frequency of this CMOS 65-nm design is f_S = 2.66 GHz.

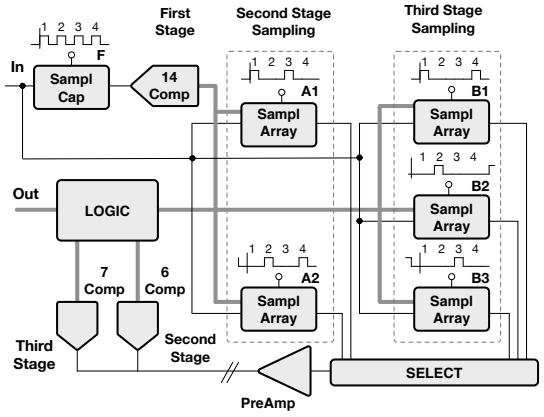

Fig. 1. Converter architecture.

II. Converter Architecture

Fig. 1 shows the block diagram of the 3-stages pipeline. It is made by a coarse, an intermediate and a fine conversion stages. In order to accommodate a given redundancy for relaxing accuracy requirements, 4 bits are solved in the coarse stage and 3 bits are solved both in the intermediate and in the fine stages. The extra-bit is shared between coarse and intermediate stage for digital correction. The coarse stage uses a normal sample and hold, while the intermediate and the fine stages use two (A_1, A_2), and three (B_1, B_2, B_3) sampling arrays made by 16 unity elements and 64 unity elements respectively. The multiple sampling arrays operate as an analog delay line since it is necessary to have a delay for getting the bits from the previous stage of the pipeline.

The coarse stage uses 14 comparators. The thresholds are nominally set at voltages corresponding to the bins ($24+n\cdot 16$), with $n=0,\cdots,13$. A thermometric zero at output identifies the bin interval $0,\cdots,32$, the thermometric one identifies $16,\cdots,48$ and so forth, as Fig. 2 shows. The comparator accuracy must be ±8 LSB, about ±16 mV for 1-V reference voltage. The margin is large enough for a properly designed comparator and reasonable clock skew. Therefore, the stage does not need calibration.

The thermometric output of the coarse stage drives the intermediate capacitive array A_i and sets its output to the mid point of the identified interval. A special preamp scheme, described in detail shortly, generates six outputs corresponding

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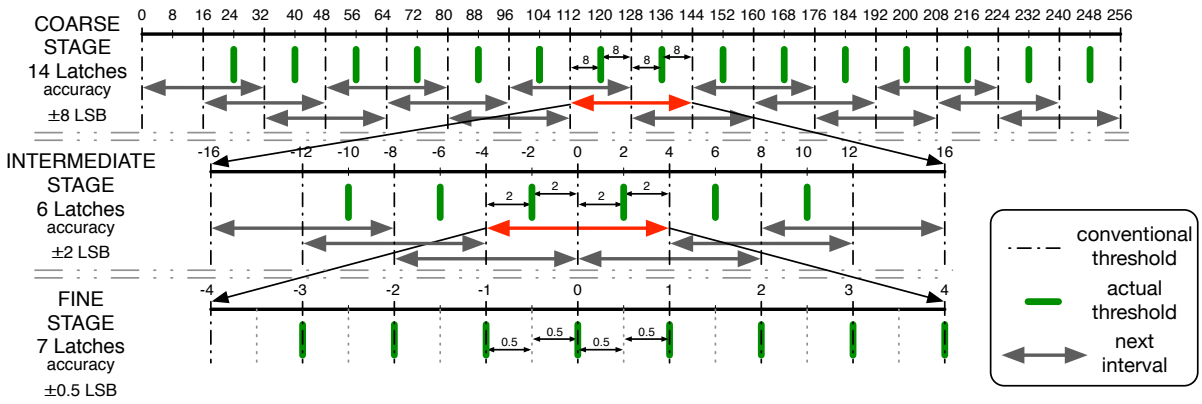

Fig. 2. Conversion algorithm.

to the nominal thresholds illustrated in Fig. 2. A bank of six latches generates a thermometric output that, along with the flash thermometric output, drives the array B_i and selects six intervals of 8 bins to be analyzed by the third stage of the pipeline. The used redundancy allows a ± 2 LSB accuracy before the preamplification. Finally, the same preamplifier is used to generate another seven outputs corresponding to the nominal thresholds for the fine stage illustrated in Fig. 2 and a bank of seven latches generates the last thermometric output. A logic block combines the outputs from all the three stages and generates the 8-bit word.

III. System Implementation

Pipeline architectures transfer the residual from one stage to another. An amplification factor relaxes the accuracy requirements of the successive stage. The limit to accuracy for conventional pipelines comes from the ADC, the DAC and the analog blocks used to generate the residual. In order to operate at very high-speed, this architecture avoids the interstage gain. Instead, it uses multiple input sampling to avoid the analog block required for the residual propagation, and generates the quantization error using the charge redistribution method commonly used in SAR architectures.

As mentioned above, the coarse conversion is carried out with a flash converter. The comparators are just latches because the required accuracy is limited. The input capacitance is very low as the input transistors of a latch can be almost at the minimum size. The subsequent stages use capacitive DAC arrays. Each thermometric output of the coarse flash alternately drives the unity capacitors of the arrays of the intermediate stage A_1 and A_2, as shown in Fig. 3(a). Those outputs also drive fourteen $4C_u$ capacitors of the arrays of the fine stage B_1, B_2 and B_3 as shown in Fig. 3(b). The intermediate conversion generates six thermometric outputs used to set six of the remaining unity capacitors of the fine stage arrays.

Fig. 4 shows the timing of each stage in a complete conversion cycle. Input is sampled simultaneously in the flash ADC input capacitance F, and in the capacitive arrays A_1 and B_1. After sampling, the flash section carries out the first conversion step. Information is then transferred to the array A_1 which completes the intermediate conversion, while a new input is sampled on F, A_2 and B_2. Finally, information is

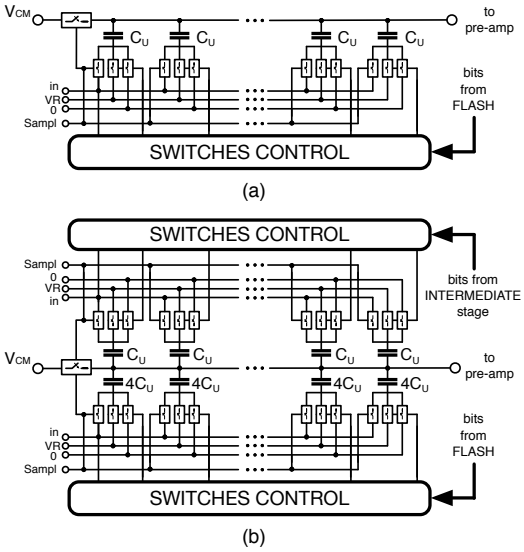

Fig. 3. Capacitive DAC arrays structure. (a) Structure of the intermediate DAC array A_i. (b) Structure of the fine DAC array B_i.

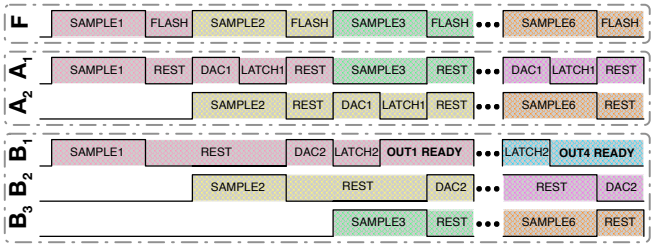

Fig. 4. Timing diagram.

transferred to the array B_1 for the fine conversion stage. The new input is sampled on F, A_2 and B_2 for similar processing. The successive sampling uses F, A_1 and B_3 and so forth. This sampling configuration repeats periodically every 6 conversion cycles.

Main issues in multi-bit per cycle converters are the thresholds generation and offset mismatch of the used comparators.

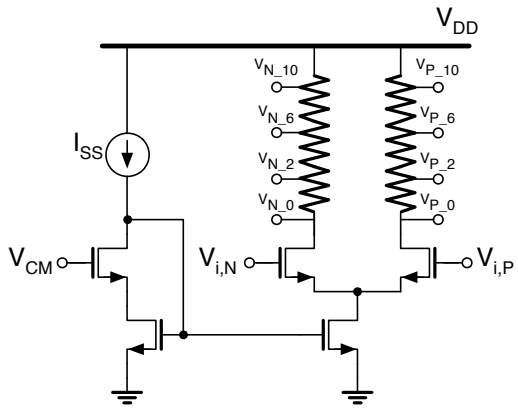

Fig. 5. Preamplifier with embedded thresholds generation.

Thanks to the relaxed accuracy required for the coarse conversion stage, the flash ADC uses a very simple structure. Thresholds are generated through a resistive string without calibration and the input is sampled directly on the input parasitic capacitance of comparators.

Since the accuracy requirements of the intermediate stage are higher than the ones of the the coarse stage, the offset mismatch of comparators causes an error that cannot be corrected by redundancy. In order to overcome this limitation, a preamplifier with multiple outputs is placed in front of the latches bank. Since the preamplifier uses the same differential pair, the mismatch error just depends on loads. As described in details shortly, loads are made by resistors whose matching accuracy is good enough for the expected resolution. The gain of the preamplifier relaxes the matching requirements of the latches. Another limit can be the offset mismatch between intermediate and fine stage. This error can cause large INL and even missing codes. Time interleaving of the preamplifier between intermediate and fine stage is the solution adopted to overcome this limitation.

IV. Preamplifier with Embedded Thresholds Generation

Fig. 5 shows the schematic diagram of the preamplifier used to give at multiple outputs the differential signals needed for the multi-bit conversion. It is a differential pair with resistive load and multiple taps. The use of outputs with same resistive load allows detecting a zero crossing. Using, for example, the outputs V_{N-0} and V_{P-2} the amplified differential input $\Delta V_{in} g_m R_L$ should compensate a shift ΔV_{02}

$$\Delta V_{0-2} \simeq \frac{I_{SS}}{2} R_{0-2} \tag{1}$$

where R_{0-2} is the resistance between the two taps V_{P-0} and V_{P-2}.

For ΔV_{in} = 2 LSB, the condition is

$$2\,LSB \simeq \frac{I_{SS}}{2g_m}\frac{R_{0-2}}{R_L} \tag{2}$$

where R_L is the average load of the two branches.

Since the transconductance of MOS transistors of the input pair in saturation is approximately proportional to $\sqrt{I_{SS}/2}$,

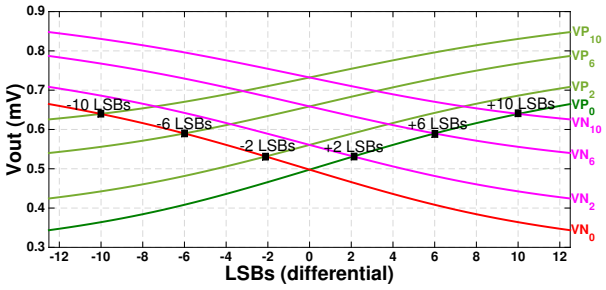

Fig. 6. Preamplifier multiple outputs for thresholds generation.

there is a value of the bias current that can obtain a value of ΔV_{0-2} detecting ΔV_{in} = 2 LSB. Using $R_{2-6} = 2R_{0-2}$ gives rise to a shift that should be compensated by 6-LSB and $R_{6-10} = 2R_{0-2}$ increases the shift for the 10-LSB detection. Notice that the gain varies due to the non linear response of the differential gain. The error can be corrected by trimming the load resistances. The circuit operates with input differential signals and incorporates the embedded generation of all the thresholds necessary to control multiple latches.

Fig. 6 shows the transistor level simulated results in 65-nm CMOS technology with $V_{DD} = 1V$ and $V_{Ref} = 1V$. The input range is [−12.5,+12.5] LSBs or [−50,+50] mV. With a biasing current I_{SS} = 600 µA, the achieved gain and bandwidth are $A_V = 4$ and $BW = 23$ GHz, respectively. As Fig. 6 shows, the crossings of output voltages occur with different common mode level. The one for equal inputs is at 0.5 V for an optimal overall response. There is a slight non-linearity caused by the differential pair. A limited variation of the common mode is irrelevant because a latch admits a given range of common mode input. The second limit is corrected by trimming resistances according to circuit simulations.

The overall accuracy depends on linearity and gain of the preamplifier. These two features limit the maximum gain for

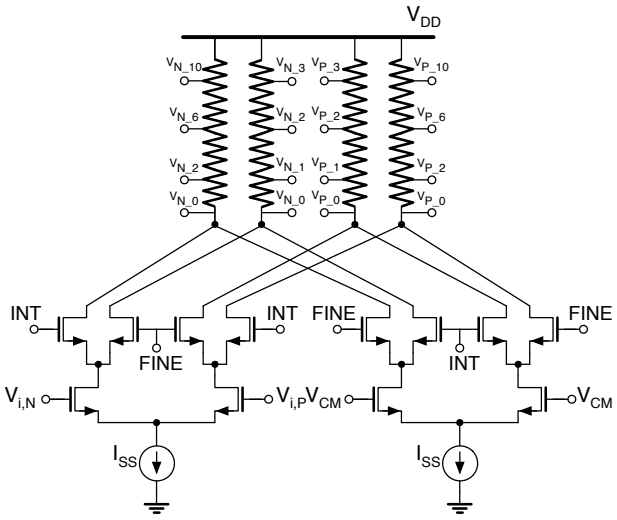

Fig. 7. Improved preamplifier with embedded thresholds generation and multiple output branches.

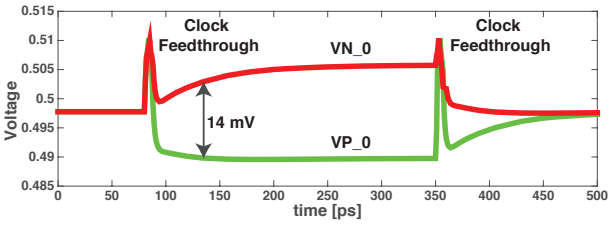

Fig. 8. Simulated reference outputs of the preamplifier fine branch with differential input voltage of ±2 mV.

large threshold differences. Having a relatively low gain for the intermediate stage is not a serious limit. On the contrary, for the fine stage having a larger gain is advisable. For this reason, this design uses two different preamplifiers with shared differential input and different output branches, as Fig. 7 shows. Each resistive branch matches the required dynamic range of the served pipeline stage.

Leaving unconnected the unused branches would push the output nodes to V_{DD}, as no current flows through them. This requests a recovery time when switching the output branches. An auxiliary differential stage overcomes the problem. A dummy structure biases the unused branch and guarantees a proper current flowing through it when unused. The inputs of the dummy differential stage are both connected to V_{CM}. Fig. 8 shows the transient response of the reference outputs of the fine branch with a differential input of ±2 mV. The figure outlines a gain of 3.5 achieved after 40 ns. Once the clock goes low, the outputs are connected to the dummy differential stage with same input at V_{CM}.

V. Comparator with Built-In Preamplification

As mentioned before, for taking advantage of the gain introduced by the preamplifier, it is necessary to use the same structure for all the arrays A_i and B_i. This would mean not to overlap DAC and latch phases in the timing schedule. Such a constraint would limit the achievable bandwidth of the ADC.

The latch shown in Fig. 9 optimizes speed and sensitivity, and allows to overlap DAC and latch phases of different stages in the pipeline configuration. This structure, studied in details

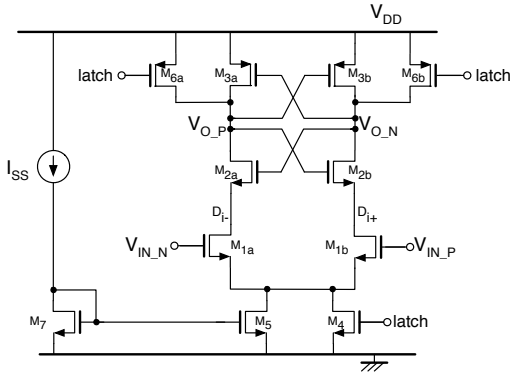

Fig. 9. Schematic diagram of the voltage comparator with built-in input sampler.

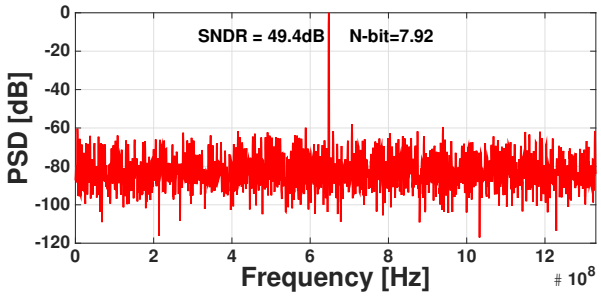

Fig. 10. Simulated output spectrum at 2.66 GS/s with a 646-MHz full scale input signal.

in [5], integrates the preamplification function into the latch itself. In the reset phase, the current I_{SS} flows through the pair M_{1a}-M_{1b} while transistors M_{2a} and M_{2b} are diode connected by the reset. The result is an amplification of the input by the square root of the aspect ratio of input transistors and the one of the diode connected load. In the latch phase, the circuit works as a conventional sense amplifier latch. The comparator starts the latch phase with its outputs already unbalanced, like in the case of a static class AB comparator. The circuit disconnects the comparator input immediately after starting the latch phase, thus allowing to change the array driving the preamplifier and obtaining an optimal timing schedule of the ADC.

VI. Simulation Results

The proposed scheme has been post-layout simulated using a 65-nm CMOS technology. The nominal supply voltage is 1 V and the input clock frequency is 2 GHz (2.66 GS/s).

Fig. 10 shows the simulated output spectrum with a full scale sinusoidal input signal at 646 MHz. The fft has 4096 points. The achieved signal-to-noise and distortion ratio (SNDR) is 49.4 dB, equivalent to 7.92 bits of resolution. The simulated total power consumption is 22.06 mW and the resulting figure of merit (FoM) is 32.4 fJ/conversion-step.

The results of this design demonstrate the possibility to achieve 8 bit of resolution and 2.66 GS/s conversion rate with a 65-nm CMOS technology. This almost corresponds to the state of the art.

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