Optimization of the Data Rate of an OOK CMOS Medical Transmitter Based on LC Oscillators

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***Abstract*—This paper presents techniques for increasing communication data rates for OOK modulated signals in the case the carrier frequency is generated by a cross-coupled pair LC oscillator. The proposed circuitry completely turns off the transmitter during the transmission of "0" bit and oscillation occurs only when the data bit is "1" to reduce power consumption. The data bit controls the steady state bias current and the operation of the oscillator. The communication data rate is limited by the turn-on and turn-off time of the LC oscillator. In order to speed up the turn-on time of the oscillator, in addition to bias current, an extra current source is used during the build-up of the oscillator. The decay time of the oscillator when the data is switched from "1" to "0" is accelerated by shortening the inductor connections. The concept is demonstrated through the design of an LC VCO in 0.18 μm CMOS technology. The LC oscillator is designed to oscillate in MedRadio band at 416 MHz frequency. Simulation results show that the proposed architecture shortens the turn-on time from 86.5 ns to 24 ns and the turn-off time from 101 ns to 5.93 ns. With the additional techniques, the maximum achievable communication data rate is increased by more than 6 times.**

I. Introduction

The advancements in design methods and improvements in fabrication techniques makes the technology as an essential part of daily life. Especially the miniaturization of the technology enables the implantable and wearable devices which can be very useful in many applications such as medical, entertainment, security, and commercial fields [1]–[4]. Recently, there is a large demand especially on medical applications of implantable systems. By means of medical implantable systems, it is possible to acquire information about several parameters such as patients body temperature, heart rate, brain activity, and other physical and chemical data. As a result of these measurements, the cause of the illness can be investigated, the recovery process can be monitored, early detection and prevention of diseases becomes possible. In order to achieve the mentioned applications, there is a need for a system which is composed of two parts: collection and transmission of the data. The data is collected by the help of various sensors and the collected data is transferred to an external base station. Since the wires limit the mobility of the patient and the penetration holes for the wires may cause the infections, wireless data communication becomes a preferable solution for the transmission of data.

Data generated by the sensor network is transferred wirelessly to an external base station by using different types of modulation techniques. During the data transmission, "0" and "1" bits can be coded by changing the signal parameters such as its amplitude, frequency, and phase. Every modulation technique has its own advantages and disadvantages. In an implantable system, in addition to the size and weight restrictions, there is also a limitation for the power budget. Accordingly, on-off keying (OOK) modulation is a promising solution for low power consumption because it does not consume power for "0" bits unlike the other modulation methods. Moreover, OOK modulation is very simple to implement in terms of the design perspective since it requires only the activation and deactivation of the oscillator. However, although OOK modulation consumes less power and has a simple structure, its data rate is reduced due to the slow nature of transitions from ON state to OFF state and vice versa. In this work, the methods for the optimization of OOK modulation in terms of data rate and their results are presented. Section II shows the oscillator structure taken as a reference for the data rate optimization. In Section III, the methods for reducing the rise and fall times of the oscillator are covered. The optimized OOK transmitter implementation and post-layout simulations are presented in Section IV and Section V concludes the work.

II. Transmitter Architecture

In order to analyse the rising and falling time of an oscillator, a cross-coupled symmetrical voltage controlled oscillator (VCO) whose schematic is presented in Fig. 1 is chosen as a reference oscillator. This type of oscillator is selected since it provides a balanced output and shows a better phase noise performance at a given power dissipation compared to the asymmetrical version of it [5]. The resonance frequency of the oscillator is determined by the tuning capacitors and the inductance of a loop antenna which is implemented as off-chip. The antenna is directly connected to the differential pins of the cross-coupled VCO. The parameters for the tuning capacitors and the loop antenna are selected such that it oscillates in MedRadio band at 416 MHz frequency.

The OOK encoded signals at the output of the oscillator is generated by turning ON/OFF the current source of the cross-coupled VCO. The modulated bias current is multiplied by a current mirror and this multiplication introduces some delay between the data and oscillator output. When the current source is switched ON, the output of the VCO starts to build up exponentially. This similar exponential behaviour of the VCO is obtained during the turn-off procedure of the oscillator. Fig. 2 shows the simulation results for the response of the oscillator designed in 0.18 μm technology to the applied data signal. Fig. 2(a) represents the message signal and Fig. 2(b) shows the output voltage response and its envelope to the data

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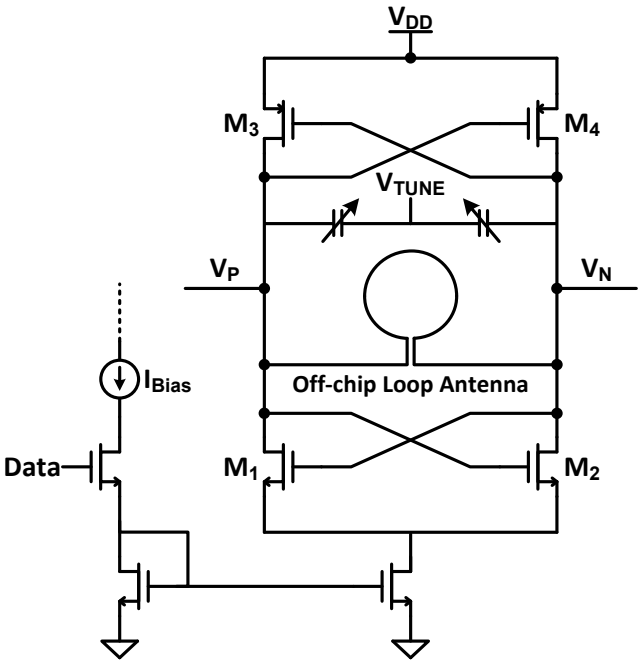

Fig. 1. Schematic of the reference cross-coupled voltage controlled oscillator.

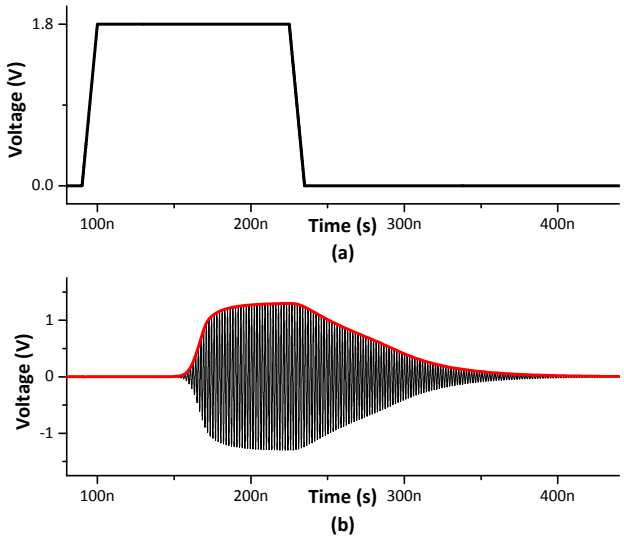

Fig. 2. (a) Applied data signal to the oscillator. (b) Simulated output response of the oscillator.

for modulated 20 μA bias current. The exponential response of the oscillator can be analysed by considering the equivalent circuit of the VCO as show in the Fig. 3 and the corresponding equivalent parameters as

$$\begin{aligned} L_{tank} &= L_{loop} \\ R_{tank} &= 1/(g_{tank} + g_t + g_L) \\ C_{tank} &= C_{NMOS} + C_{PMOS} + C_L + C_{load} + C_V \end{aligned} \tag{1}$$

where g_{tank} is the sum of the output conductance of NMOS and PMOS, g_t is the parasitic conductance of the tuning

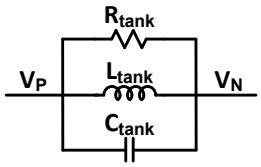

Fig. 3. Equivalent circuit of the cross-coupled VCO.

capacitors, g_L is the parasitic conductance of loop antenna, C_{NMOS} and C_{PMOS} are the parasitic capacitance of cross-coupled transistors, C_L is the parasitic capacitance of the loop antenna, and C_{load} is the parasitic capacitance at the load of the oscillator [6]. The waveform of the oscillator output, $V_{out} = V_P(t) - V_N(t)$, for a unity bias current can be expressed by [7]

$$V_{out} = \frac{e^{-\xi\omega_0 t}}{\sqrt{1-\xi^2}} \cos\left[\omega_0\sqrt{1-\xi^2}t - \tan^{-1}\left(\frac{\xi}{\sqrt{1-\xi^2}}\right)\right] \tag{2}$$

where

$$\xi = \frac{1/(2R_{tank}C_{tank})}{1/\sqrt{L_{tank}C_{tank}}} \tag{3}$$

The equation (2) and (3) expresses that the time constant of oscillation envelope is $2R_{tank}C_{tank}$ while ω_0 is stated as $1/\sqrt{L_{tank}C_{tank}}$. This relation shows that the smallest rising time/falling time of the oscillator can be achieved by the smallest R_{tank}. Since R_{tank} includes the output conductance of the cross-coupled transistors, increasing bias current increases the output conductances and decreases equivalent resistance of the tank, R_{tank}. However, increasing bias current also increases the power consumption of the VCO. Therefore, in this work, higher bias current is applied during the rising time of the oscillator in order to obtain faster switching with keeping the additional power consumption minimum. For the falling time of the oscillator, the equivalent resistance of the tank is minimized by adding a very small resistance in parallel to R_{tank}. The details of these methods for increasing the switching time of the oscillator are presented in the next section.

III. Fast Switching Oscillator Topology

A. Optimization of Rising Time

Fig. 4 shows the OOK modulated data signal for a conventional solution and possible methods used to speed-up the rising of the oscillator output. Fig. 4(a) depicts the conventional OOK modulated signal. It remains high from time t_1 to t_2, an interval that must be larger than the delay time featured in Fig. 2(b). The other two figures show waveforms with boosted currents at the turn-on time. Fig. 4(b) foresees an extra constant current. Fig. 4(c) uses a pulse fading exponentially added to the bias current. Since the current required to sustain oscillation has a value lower than the one necessary to start oscillation the current amplitude after the pulses can be brought close to the minimum. The boosted current in Fig. 4(b) requires another constant current source for the biasing and monostable circuit that controls the timing of the start-up current. As an alternative

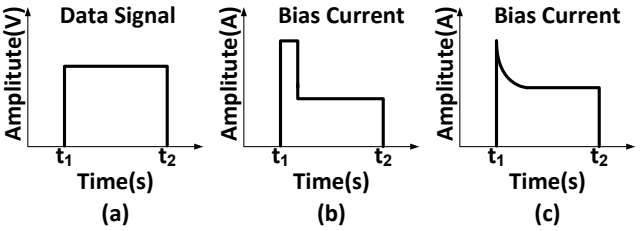

Fig. 4. (a)Applied data signal to the oscillator. Modulated bias current with additional (b) constant current and (c) exponentially decaying current.

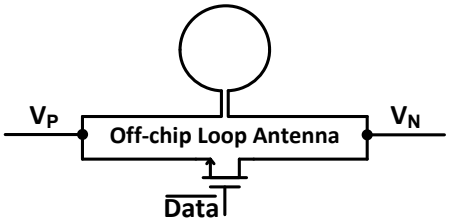

Fig. 6. Schematic of the switch added to the differential output pins of the oscillator.

to the constant biasing current, an exponentially decaying bias current is proposed since it requires fewer components to generate current and to control the time constant of the decay. Fig. 5 shows the required circuit for the generation of the current in Fig. 4(c).

A differentiator circuit generates the decaying bias current. The network composed of R_{bias} and C_{bias} creates the derivative of the inverted data signal at the gate of the PMOS transistor and the transistor creates a current proportional to the derivative. Accordingly, the generated current rises up with rising of the data signal and reaches a peak when there is no more change in the data signal. The peak of the generated current by the PMOS transistor strongly depends on the slope of the data signal when it is rising. After the data signal reaches its stable form, the current starts to decay with time constant of $R_{bias}C_{bias}$. Since the peak current depends on the rise time of the pulse controlling the gate of the p-channel transistor and the decay depends on the $R_{bias}C_{bias}$ time constant, a suitable control of variables leads to an optimal rise time of the oscillator while keeping limited the extra power consumption.

B. Optimization of Falling Time

As evident from Fig. 2(b) the fall time also limits the speed of data transmission. The solution used here foresees the simple use of a switch controlled by the data. Thanks to the low on-resistance of the switch the time constant of the tank $R_{tank}C_{tank}$ becomes very small, thus stopping the oscillation in a very short time. Therefore, a switch with small ON resistance is connected to the differential output pins of the oscillator as shown in Fig. 6. The added switch introduces a small capacitance at the output of the oscillator which causes a shift in the oscillation frequency. Since the frequency change is very small, the shift can be compensated by the tuning voltage of the varactors. The dimensions of this transistor have been chosen so that it stays in normal operation. The optimized oscillator with respect to rise and fall times of the output and its simulation results are presented in the next section.

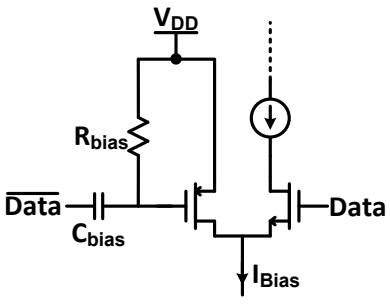

Fig. 5. Schematic for generating exponentially decaying current.

IV. OOK Transmitter Implemantation and Post-Layout Simulation Results

The optimizations for rising and falling times of the oscillator output is applied to the reference circuitry and represented in Fig. 7. The optimized VCO is designed in 0.18 μm technology. The constant current bias is kept the same in order to obtain the same steady state amplitude with the reference circuitry. The time constant $R_{tank}C_{tank}$ for the decaying bias current is set to 4.5 ns for optimization of data rate and power consumption. The post-layout simulated waveform of the reference and optimized VCO is shown in Fig. 8 and Table I summarizes the simulation results.

The time between the time that data signal reaches 10% of its maximum voltage to time that oscillation envelope crosses its 90% of steady state amplitude is measured as rise time. The fall time is measured as the falling of the oscillation from 90% to 10% of its maximum value. Achievable maximum data rate is calculated by $k/(\text{Rise Time} + \text{Fall Time})$ with the

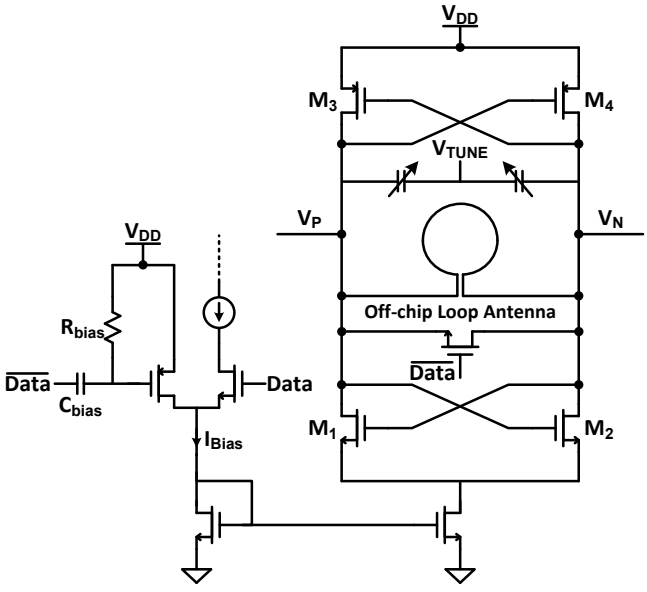

Fig. 7. Schematic of the optimized cross-coupled voltage controlled oscillator.

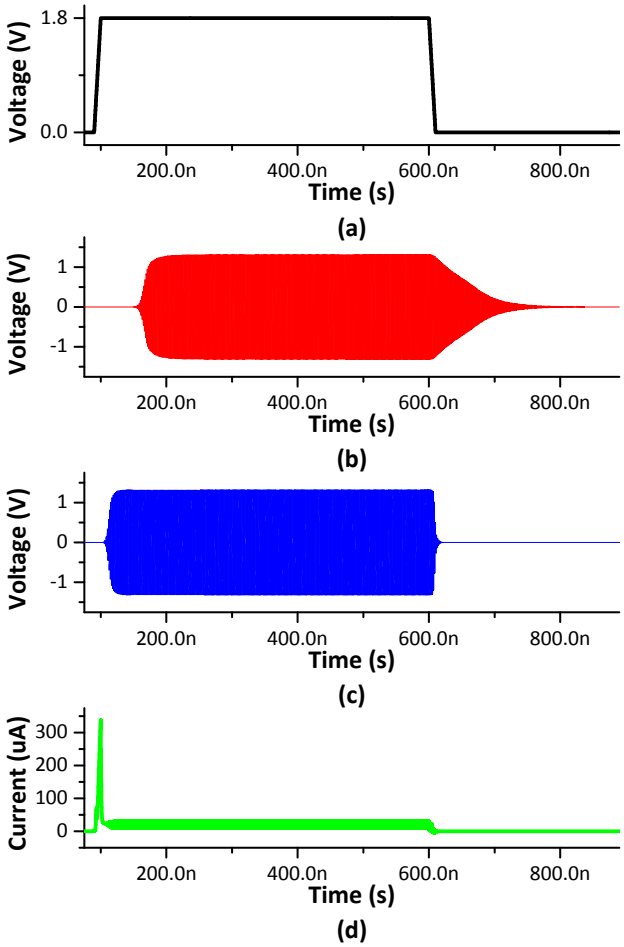

Fig. 8. (a) OOK modulated data signal. (b) Output waveform of the reference VCO. (c) Output waveform of the optimized VCO. (d) Generated bias current for the VCO.

assumption of same durations for "0" and "1" bits where k indicates the margin for pulse width. DC power consumption of the VCO is calculated by assuming that the data is uniformly distributed as "..1010.." and ratio of the energy consumption and the data rate gives the energy efficiency of the VCO.

The proposed optimization improves the rising time and the falling time of the oscillator significantly. The maximum data rate achieved by the oscillator increased more than 6 times. Although there is an increase of 136 μW in the DC power consumption which corresponds to 28% increase, the energy efficiency is improved by 4.8 times. Fig. 9 shows the optimized performance of the oscillator with 25 Mbps data rate. This

TABLE I. SUMMARY OF THE SIMULATION RESULTS

Parameters	Reference VCO	Optimized VCO
Rise Time (ns)	86.5	24.0
Fall Time (ns)	101	5.93
Maximum Data Rate (Mbps) [k=0.75]	4	25
DC Power (μW)	473	609
FoM (pJ/bit)	118	24.4

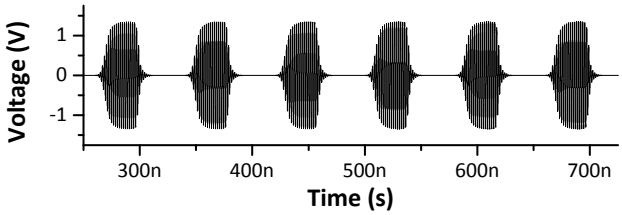

Fig. 9. Output waveform of the oscillator with 25 Mbps OOK signal

optimization methods provide major increase in the timing properties of the oscillator by introducing a few additional components.

V. CONCLUSION

This paper presents methods for optimization of the rise and fall times of a cross-coupled pair LC voltage controlled oscillator for high communication data rates. The OOK is taken as a modulation type of communication since it consumes power only for "1" bits. The rising time of the oscillator is decreased by additional bias current during the start-up and the fall time of the oscillator output is reduced by shortening the differential output pins. The proposed techniques are demonstrated with a cross-coupled LC VCO designed in 0.18 μm technology. Post-layout simulation results show that the total time for rising and falling is improved by more than 6 times. Although the optimization introduces additional power consumption, the energy efficiency is increased about 4.8 times. This optimization is suitable for low power, high data rate OOK communication. This method can be extended to any type of LC oscillator.

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