HIGH-FREQUENCY IMPLEMENTATION OF SIMPLE SC TRANSFER FUNCTIONS

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ABSTRACT
The design of simple switched-capacitor circuits suitable for high-frequency operations is presented. Emphasis is placed on the use of single-stage operational amplifiers with moderate dc gain, but with very high bandwidth. Simulation results are included.

INTRODUCTION
Despite the fast technological progress in the last twenty years, very accurate processing of high-frequency signals is still a difficult task. The speed limitation of analog switches and active elements are the main factors responsible for placing upper frequency limits to the processing of signals directly in the analog domain by either continuous-time or SC techniques. While analog switches can be made fast by a suitable dimensioning and driving, active elements can only be made fast at the cost of a low dc gain. The existing tradeoff between speed and gain makes it impossible to achieve high bandwidth and high gain simultaneously.

Digital signal processing of analog signals is increasingly becoming an attractive alternative in many applications due to the rapid advances in digital VLSI circuit technology. In this case, however, limitations arise from the availability of accurate and fast A/D converters. Generally, fast A/D converters have poor resolution because of the limited high-frequency performances of their analog components. However, through a suitable combination of parallel processing and subband analysis, an increase in the achievable resolution may result. In such a scheme the input (analog) signal is initially split into different subbands by the use of a filter bank. Then, the signal in each band is converted into digital form and the resulting digital signal is suitably processed [1]. With such a solution, and more generally in all cases where an analog pre-processing is required before the digital conversion takes place, the main problem becomes the design of accurate analog front ends. A solution to this problem can be successfully found if only simple transfer functions are used. Typically, these transfer functions are of the form \((1 - z^{-1})\) and \((1 + z^{-1})\).

This paper presents a novel circuit technique for the SC implementation of such transfer functions with a reduced dependence on the finite gain of the active elements used. The objective is to use single-stage operational amplifiers with moderate dc gain, but with very high bandwidth.

FINITE GAIN ERROR REDUCTION TECHNIQUES
Precise switched-capacitor circuits always require the use of operational amplifiers. The clock frequency in sampled data systems must be larger than twice the signal bandwidth and, in order to avoid errors coming from the speed limitation, the clock frequency must be at least four times smaller than the gain-bandwidth product of the operational amplifier. As a consequence, for high-frequency input signals the bandwidth of the operational amplifiers used in SC circuits must be very high.

An operational amplifier can be made fast by increasing the bias current or, in order to reduce the non-dominant node capacitances, by reducing the transistor dimensions. However, the output impedance of the transistor decreases and the dc gain is lowered.

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In order to get high accuracy in high-frequency analog processors it is necessary to use circuit techniques capable of reducing the finite gain effects. Several techniques have been proposed in the past. Unfortunately, all of them are effective only in a given frequency range and, therefore, they are not suitable for large bandwidth signals.

All finite gain compensation techniques can be explained making use of what we call “predict and correct” approach. The finite gain causes an error which, if properly predicted in one phase, can be used in the following phase to reduce its effect. A proper estimation of the error is the non-zero voltage of the virtual ground. In the integrator of Fig. 1 [2], the virtual ground voltage is used to predict and correct the finite gain dependence.

While the injecting capacitor $C_1$ is discharged (during phase 2) a dummy capacitor $C_a$ is precharged to the virtual ground; the output voltage at the previous phase is held by capacitor $C_3$. If the output variation in one clock is small enough, the voltage stored on $C_a$ gives a good estimate of the error in the successive injection phase 2. During phase 2 the capacitor $C_a$ is used as a level shift to correct the error. Incidentally it is worth noting that the capacitance $C_3$ is a capacitive load to the operational amplifier during the injection phase, thus alleviating the speed reduction of the circuit. Moreover, the correction of the error is now dynamic, i.e., frequency dependent. Similar results have been obtained in the analysis of the operation of other solutions [3].

**IMPLEMENTATION OF $1 + z^{-1}$ AND $1 - z^{-1}$**

These simple transfer functions find a wide range of applications in signal processing [1], [4]. Using the approach described in the previous section, it is possible to implement very simple transfer functions such as $1 + z^{-1}$ and $1 - z^{-1}$. In order to implement them, a unit delay, an adder and a subtractor are necessary and can be realized by the “predict and correct” method as briefly described below.

The circuit in Fig. 2 implements $1 + z^{-1}$, and using the phases indicated inside the parentheses $1 - z^{-1}$ results, as well. The input signal is sampled and stored in the two capacitors of the lower branches, and injected, during phase 2B, into the virtual ground. The capacitor $C_a$ is charged with the prediction of the error and, as in Fig. 1, used to correct the error due to the operational amplifier finite gain. Similarly, the charge injected by the upper two branches, which is a delayed version of the input signal, has a small dependence on the finite gain.

The unit delay $z^{-1}$ is realized by the circuit in Fig. 3, which is also gain compensated as follows. During phase 1 the capacitor $C_1$ is precharged with the input voltage, and during phase 2 it is connected around the operational amplifier in a feedback configuration. Because of the operational amplifier finite gain, the output voltage is not equal to the input. This error is equivalent to the virtual ground voltage which is stored in $C_a$. During phase 1 this voltage is then used to correct the error.

As an example of application of these transfer functions, we show in Fig. 4 a two-stage, tree-structured,
Simulation Results

In order to verify the effectiveness of the compensation scheme described here, extensive simulations have been performed with the circuit of Fig. 2. Some of the results obtained are presented in Fig. 5 for the circuit implementing the transfer function $1 + z^{-1}$, and using operational amplifiers with a dc gain equal to 200. Observe that the frequency response of the compensated circuit is essentially the same as that of the ideal circuit having operational amplifiers with infinite gain. Also shown in Fig. 5 is the simulated frequency response of the circuit without compensation.

Figure 5. Simulated frequency responses obtained with the circuit of Fig. 2 implementing $1 + z^{-1}$.

Figure 6 shows the simulated frequency responses (ideal, compensated, and uncompensated) of the lowest frequency band of the filter bank implementation of the Hadamard Transform in Fig. 4, corresponding to the transfer function of the upper branches of the tree structure. As in the case of Fig. 5, the error is substantially smaller for the compensated approach than for the uncompensated one. Observe that the compensation scheme is particularly important here, since the filters are connected in cascade. Thus, the accumulation of errors due to the finite gain of the operational amplifiers inside each uncompensated filter, resulting from the signal being transferred from one stage to another of the tree, may not be tolerable. Moreover, in an analysis/synthesis arrangement, the conditions for perfect signal reconstruction can no longer be satisfied.

CONCLUDING REMARKS

A design method of switched-capacitor (SC) circuits suitable for high-frequency operations has been introduced.
Figure 6. Simulated frequency responses of the lowest frequency band of the filter bank implementation of the Hadamard Transformer in Fig. 4.

Emphasis has been placed on the use of simple single-stage operational amplifiers with moderate dc gain, but with very high bandwidth, so that the use of high clock rates is possible. Simulation results obtained with simple transfer functions have been shown. The method can be extended to implement higher order FIR SC filters.

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REFERENCES


