A NOVEL CMOS INTERFACE FOR OXYGEN SENSORS

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ABSTRACT

This paper describes a CMOS interface for an oxygen sensor. It provides a differential to single-ended conversion with a good common mode rejection, a proper level shifting and an accurate voltage gain. The paper presents design considerations and measurements performed on an integrated test structure. The variation of the large-signal voltage gain is kept within ±10 % when the input common mode voltage ranges from −0.5 V to 1.5 V. The differential nonlinearity is better than −6 % to +2 % over an input differential signal range of ±0.5 V. These results meet the specifications required for automotive applications.

1. INTRODUCTION

An oxygen (or lambda) sensor is an electrochemical cell capable of detecting the composition of the exhaust gases of a vehicle. It is mounted in the exhaust pipe and senses the difference in oxygen content between the atmosphere and the exhaust gases. When inserted in a control loop, it fixes the correct stoichiometric air-fuel ratio of the mixture supplied to the cylinders of the engine.

The difference between the real air-fuel ratio and the stoichiometric one is expressed with the so-called factor λ:

\[ \lambda = \frac{\text{air/fuel (real)}}{\text{air/fuel (stoichiometric)}} \]  

(1)

The sensor output voltage \( V_g \) as a function of \( \lambda \) is shown in Fig. 1.

One of the main problems to be solved in designing the electronic interface between the sensor and the processing system, is related to the fact that these can have different ground references. The difference may be as large as ±1 V. Therefore, it is necessary to handle signals ranging very close to ground or even below the ground of the processing system. The interface should provide differential to single-ended conversion, accurate voltage gain, satisfactory linearity and level shifting around a proper value. The interface should also be capable of detecting short or open sensor connections. Finally, a very high input resistance should be provided.

A bipolar integrated interface with similar features has already been reported [1]. This interface, however, requires the use of two supply voltages (12 V and 5 V) and needs factory trimming to obtain an accurate voltage gain.

To overcome the above problems, a new fully CMOS system was designed. The complete block diagram of the developed interface is shown in Fig. 2. It is made up of the cascade of a differential to single-ended converter and level shifter (B1), a precision amplifier (B2) and a low-pass filter which rejects high-frequency noise (τ = 10 ms).

This paper describes the design and the realization of block B1, which is the most critical one in the system. Measurements carried out on an integrated test chip show that the circuit meets the required specifications of voltage gain and linearity for an input differential signal with an amplitude as large as ±0.5 V and an input common mode signal ranging from −0.5 V to 1.5 V.

2. CIRCUIT DESCRIPTION

The differential to single-ended interface is made up of a transconductance stage followed by a transresistance stage (Fig. 3). The nominal value of the supply voltage \( V_{DD} \) is 5 V.

The first stage performs the differential to single-ended conversion. Two input matched transistors (M1 and M2) are forced to work in the triode region by two local feedback loops, which keep their drains at a proper voltage. The input signals, applied to the gates of M1 and M2, are \( V_{G1} = V_{cm} + V_{in} \) and \( V_{G2} = V_{cm} + \frac{1}{2} V_{in} \) (\( V_{in} \) and \( V_{cm} \) are the differential and the common mode components, respectively). In a first approximation, the current-voltage characteristic of transistors M1 and M2 is expressed by

\[ I_D = \mu C_{ox} \left( \frac{W}{L} \right) V_{DS} \left[ V_{GS} - V_T - \frac{1}{2} V_{DS} \right] \]  

(2)

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Since the drain-to-source voltages of \( M1 \) and \( M2 \) are equal, the difference in current \( \Delta I = I_{D2} - I_{D1} \) is

\[
\Delta I = -\mu C_{ox} \left( \frac{W}{L} \right)(V_{GS1} - V_{GS2})V_{DS} = -\mu C_{ox} \left( \frac{W}{L} \right)V_{in}V_{DS}
\]  

(3)

\( \Delta I \) is then proportional to the differential input signal \( V_{in} \), and in a first approximation it is independent of the input common mode signal. A cascade current mirror, which provides excellent current matching [2], is used to obtain the current difference \( \Delta I \) at the output of the stage.

The current \( \Delta I \) is then converted into a voltage by the transresistance stage. Its circuit configuration is equal to the one in the transconductance stage. Corresponding components are matched. As a result, the transconductance and the transresistance circuits have a complementary behaviour and the voltage gain of the differential to single-ended converter is very close to unity. Therefore, no trimming is needed to obtain the required precision in the voltage gain of the interface.

Blocks A1–A5 are conventional two-stage operational amplifiers with internal pole-splitting compensation. Amplifiers A1–A4 keep the drain voltages of \( M1, M2, M9, M10 \) approximately 200 mV below \( V_{DD} \). The operational amplifiers were designed to accept an input common mode signal that can be as large as 4.8 V.

The open-wire condition is detected by connecting a p-channel microcurrent source to the non-inverting input of the interface (Fig. 2). In normal operating conditions, the microcurrent is injected into the internal resistance of the sensor (typical operating value < 1 kΩ), giving rise to a negligible input offset voltage. When the connection between the sensor and the non-inverting input is open, the latter is pushed to \( V_{DD} \). The processing system senses the resulting interface output voltage and detects the erroneous condition.

The feedback loop including amplifier A5 sets the quiescent output voltage at the desired value \( V_R \). The loop also keeps the voltage at the output nodes of the transconductance and the transresistance stage at a value that ensures the best mirroring factor for the cascode current mirrors at zero input voltage.

As required, the proposed structure has a very high input resistance.

3. ANALYSIS OF NONIDEALITIES

A more accurate analysis of the circuit means taking into account the dependence of the effective electron mobility \( \mu \) on the gate-to-source voltage \( V_{GS} \). Equation (2) becomes:

\[
I_D = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} C_{ox} \left( \frac{W}{L} \right)V_{DS} \left[ V_{GS} - V_T - \frac{1}{2}V_{DS} \right]
\]  

(4)

where \( \mu_0 \) is the zero-field carrier mobility and \( \theta = \beta_0 \mu_{ox} \) is the mobility degradation coefficient. \( \mu_{ox} \) is the gate oxide thickness and \( \beta_0 \) ranges typically from 0.001 to 0.005 μm/V [3].

Let us first consider the dependence of the circuit behaviour on the input common mode voltage \( V_{cm} \), by assuming that the differential input signal is negligible (\( V_{in} \approx V_{cm} - V_{DD} \)). The current through transistor \( M1 \) (\( M2 \)) is

\[
I_{D1(2)} = K_0 V_{DS} \left[ V_{cm} - V_{DD} - V_T - \frac{1}{2}V_{DS} + (\pm) \frac{1}{2}V_{in} \right]
\]  

(5)

where \( K_0 = \left( \frac{W}{L} \right) \frac{\mu_0}{1 + \theta(V_{cm} - V_{DD} - V_T)} \) and \( C_{ox} \). The current difference \( \Delta I = I_{D2} - I_{D1} \) results

\[
\Delta I = -K_0 V_{DS} V_{in} = - \left( \frac{W}{L} \right) \frac{\mu_0}{1 + \theta(V_{cm} - V_{DD} - V_T)} \frac{C_{ox} V_{DS} V_{in}}{L}
\]  

(6)

Therefore, the current \( \Delta I \) at the output of the transconductance stage shows a slight dependence on the input common mode voltage \( V_{cm} \). In contrast, the transresistance stage does not introduce any dependence on \( V_{cm} \) since the gate-to-source voltages of \( M9 \) and \( M10 \) are independent of it. Thus, the dependence of the converter output voltage on \( V_{cm} \) remains affected ideally only by the contribution of the transconductance stage. From equation (6), for a 3-μm process with \( \theta = 0.055 \) V⁻¹ and \( V_T = -1 \) V, the overall variation in the slope of the converter transfer characteristic (\( V_{out} \) vs \( V_{in} \)) is expected to be within ±5 % when \( V_{cm} \) ranges from -0.5 V to 1.5 V. To improve common-mode rejection performance, some compensation can be accomplished by ensuring an adaptive adjustment of the drain-to-source voltage of transistors \( M1 \) and \( M2 \). This can be obtained by making the bias voltage which sets the drain-to-source voltage of these transistors dependent on the input common mode signal. This solution has not been used in the circuit presented as its expected performance meets specifications.
In order to evaluate nonlinearities, the behaviour of the circuit when an input differential signal is applied must be considered [4]. If the fractional term in equation (4) is expanded to a Taylor series in respect of $V_{DS}$ around the quiescent point $(V_{cm} - V_{DD} - V_T)$, the following expression is obtained:

$$I_D = K_0 V_{DS} \left[ V_{cm} - V_{DD} - V_T \right] - \frac{V_{DS}}{2} + a_1 (V_{in}/2) + a_2 (V_{in}/2)^2 + a_3 (V_{in}/2)^3 + ...$$

(7)

where $a_1 = 1$, $a_2 = \frac{\theta}{1 + \theta (V_{cm} - V_{DD} - V_T)}$, and $a_3 = \frac{\theta^2}{(1 + \theta (V_{cm} - V_{DD} - V_T))^2}$. With the above value of $\theta$ and with the worst-case value of $V_{cm}$ ($1.5$ V), $a_2 = 0.05$ V$^{-1}$ and $a_3 = 0.0025$ V$^{-2}$.

The current $\Delta I$ is given approximately by

$$\Delta I = -2 K_0 V_{DS} \left[ a_1 (V_{in}/2) + a_3 (V_{in}/2)^3 + ... \right]$$

(8)

Therefore, in the transconductance stage output current even-order terms are cancelled, and third-order nonlinearities become the dominant ones.

The transconductance of the stage is

$$g_m = \frac{\partial \Delta I}{\partial V_{in}} = g_{m0} \left[ 1 + \frac{3}{4} a_3 (V_{in})^2 + ... \right]$$

(9)

where $g_{m0} = -K_0 V_{DS}$ is the transconductance value in quiescent conditions. Thus, a variation which is as small as a fraction of percent is to be expected for the value of the transconductance of the first stage over the whole input differential voltage range ($\pm 0.5$ V).

The nonlinearities introduced by the transresistance stage can be analyzed in a similar way. While the gate-to-source voltage of $M10$ changes as a function of current $\Delta I$, the gate-to-source voltage of $M9$ is kept constant. Thus, when the current $\Delta I$ is injected, both even and odd-order nonlinear terms are introduced into the output voltage of the stage. The second-order term ends up being dominant and a distortion of a few percent is expected.

4. MEASURED PERFORMANCE

The proposed interface circuit was designed and optimized using the PRECISE simulation program [5], and then integrated with a conventional 3-μm single-metal double-polysilicon CMOS technology. The active area of the integrated test chip (Fig. 4) is about 2.4 mm$^2$.

$I_{ref}$ was set equal to 10 μA. The quiescent current consumption of the circuit was 220 μA with the worst-case value of $V_{cm}$ ($-0.5$ V).

Fig. 5 shows the output current $\Delta I$ of the transconductance stage when an input differential signal ranging from $-0.5$ V to $+0.5$ V is applied ($V_{cm} = 1.5$ V). The corresponding overall variation of the small-signal transconductance is within $-0.3\% \pm 0.15\%$ over the full range of $V_{in}$.

Fig. 6 shows the output voltage of the transresistance stage, when a current ranging from $-1$ μA to $1$ μA is injected as an input. The small-signal transresistance has an overall variation which is within $-5\% \pm 0.5\%$.

These measurements confirm that the nonlinearities of the differential to single-ended interface are mainly due to the transresistance stage.

The global transfer characteristic of the converter, $V_{out}$ vs $V_{in}$, is shown in Fig. 7 ($V_{cm} = 1.5$ V). The small-signal voltage gain is equal to 1 with an overall variation which is within $-6\% \pm 2\%$.

A common mode signal ranging from $-0.5$ V to $1.5$ V was then superimposed on an input differential signal with an amplitude of $0.5$ V. The resulting transfer characteristics are shown in Fig. 8. The variation of the large-signal voltage gain is within $\pm 10\%$ over the whole input differential and common mode ranges, thus meeting the specifications required of an oxygen sensor interface.

REFERENCES


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Fig. 1 - Sensor output voltage as a function of $\lambda$.

$V_{\text{max}} = 800-1000 \text{ mV}$
$V_{\text{min}} = 100 \text{ mV}$

Fig. 2 - Block diagram of the CMOS interface.

Fig. 3 - Circuit diagram of the differential to single-ended converter.

Fig. 4 - Photograph of the integrated test structure.

Fig. 5 - Measured output current of the transconductance stage, $\Delta I$, as a function of the input differential voltage $V_{\text{in}}$ ($V_{\text{cm}} = 1.5 \text{ V}$).

Fig. 6 - Measured output voltage of the transresistance stage, $V_{\text{out}}$, as a function of the input current $\Delta I$.

Fig. 7 - Measured transfer characteristic of the differential to single-ended converter ($V_{\text{cm}} = 1.5 \text{ V}$).

Fig. 8 - Measured transfer characteristics of the converter ($V_{\text{cm}} = -0.5 \text{ V to 1.5 V; step = 0.5 V}$).