QMFR-BASED A/D CONVERTERS: OVERVIEW AND NEW RESULTS

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ABSTRACT

This paper provides an overview of A/D converters incorporating a quadrature mirror filter bank. The major difference existing between these and the time-interleaved architectures (both make use of an array of A/D converters) is that, in the former case, suitable bandpass filters are used before and after the quantizers, reducing the effect of quantization noise produced by the array of A/D converters, as shown here. The noise introduced by the switched-capacitor filters, which implement the analysis filter bank in the QMFR-based data converters, is estimated. Simulation results obtained with images are presented.

INTRODUCTION

High-speed A/D conversion can be achieved by using a parallel array of M A/D converters (sub-converters) interleaved in time as illustrated in Fig. 1, each of them working at a speed (1/M)-th of the input sampling rate. The potential advantages of this method are substantial reduction in die area and power consumption, when compared to flash converters. It has been shown [1] that by using an array successive approximation A/D converters, the speed of a flash converter can be obtained with considerable savings in the die area.

One of the drawbacks of the interleaved architecture is the distortion introduced by the demultiplexer when sampling high-frequency input signals. This is due to the time uncertainty (jitter) of the sample-and-hold circuit preceding each sub-convertor, when switching from sampling to the hold mode, leading to a corresponding uncertainty in the stored value. Very accurate sampling intervals are then required to assure sufficient accuracy, since even a small deviation of the sampling interval may cause significant error [2]. A second major problem is due to mismatches among the sub-converters creating aliasing distortion in the resulting digital output [3].

A new A/D conversion architecture that makes use of an array of low-speed A/D converters (sub-converters) and a quadrature mirror filter (QMF) bank to implement high-speed A/D converters has been introduced in [4]. While it is a natural extension of the time-interleaved A/D converter, the new structure incorporates the advantages of sub-band coding and reduces considerably the effect of mismatches among the sub-converters at a little additional cost.

A block diagram of the QMFR-based A/D converter is shown in Fig. 2. The analog input signal samples are initially split into M frequency bands by a switched-capacitor (SC) analysis filter bank, creating M sub-band signals. These signals are first down-sampled and then passed through the sub-converters, which work at a speed (1/M)-th of the input sampling rate. Finally, the digital outputs of the sub-converters are up-sampled and then added up, after being filtered by a synthesis filter bank, producing the digital converted value. As mentioned earlier, the time-interleaved A/D converter is a special case of the scheme of Fig. 2 with |K| = 2, and P(x) = x^[M-1-k],

for k = 0, 1, ..., M - 1.

The accuracy of each sub-convertor is in practice limited by random errors in its circuit components, and, therefore, mismatches among the sub-converters are inevitable. As a result, the output spectrum is corrupted by aliased components of the input signal. The use of sharper roll-off filters, on the other hand, reduces substantially such distortions, by attenuating each aliased component [4]. Since the input signal is decomposed into several contiguous frequency bands, a specific sub-convertor can be assigned to each band. Sub-converters with higher resolution can be assigned to those bands in which higher signal energy is concentrated. In this way, the quantization noise produced in one band is confined to that band and does not influence any other band.

This new scheme has been simulated on a computer and tested in the laboratory using discrete elements. The simulation and experimental results have verified the good performance of the proposed approach [4]. Efficient implementation of the SC filters that realize the analysis filter bank has been addressed in [5], where the design of SC circuits suitable for high frequency operations has been discussed. There the emphasis has been placed on the use of simple single-stage operational amplifiers with moderate dc gain, but with very high bandwidth.

THE QMF BANK

The QMF bank is designed to cancel (or reduce) three types of distortion, namely aliasing, phase distortion and magnitude distortion. Since the frequency responses of the analysis filters H(x) overlap, aliasing distortion occurs due to the down-sampling stage. This type of distortion, however, is perfectly cancelled (assuming that no transmission error takes place when the sub-band signals are transferred from the down-samplers to the synthesis filters) by properly choosing the synthesis filters [6]. The analysis and synthesis filters may introduce magnitude or phase distortions, depending on the type of filter used (FIR or IIR). Phase distortion can be eliminated by using linear phase FIR filters. In this case the magnitude distortion can be minimized through the use of a computer-aided optimization algorithm in the filter design [6]. If IIR filters are used in the scheme of Fig. 2, then the magnitude of the Fourier transform of the output digital signal (n/T) is identical to the magnitude of the Fourier transform of the analog (sampled-and-held) input signal u(nT). In applications where phase distortion can be tolerated, this approach leads to a much smaller circuit complexity [1]. If linear phase is also needed, however, then additional allpass stages are needed for phase equalization. Simulation and experimental results obtained with QMF-based con-

1 Reznick and Foss [7] and Barlow [8] have reported the results of analytical and experimental study of the impact of using IIR filters for the band-splitting function in tree-structured sub-band coders for speech.
filter of the QMF bank, we have
\[ SNR_{qur}^b = SNR_{qur}^a + 10 \log_{10} M. \]

The increase in the number of effective bits of resolution is, therefore, given by
\[ \nu_{qur} = \log_{10} M. \]

The above is a special deterministic situation in which the input signal is composed of sinusoids, one inside each passband of the QMF bank. A more interesting situation, however, is the case of a wideband signal input, which is considered next.

**Wideband Signal Input**

Let us assume that a wideband signal having average power \( \sigma_w^2 \) is input to a time-interleaved converter having two sub-converters (\( M = 2 \)). Let us assume also that each sub-converter has a full-scale voltage \( V_{fs} \). As before, the quantization noise power \( \sigma_q^2 \) is the same as that produced by each sub-converter, and is given in Eq. 1. The signal-to-noise ratio is, therefore,
\[ SNR_{w}^q = 10 \log_{10} \frac{\sigma_w^2}{\sigma_q^2}, \]
where the superscript "w" denotes the case of a wideband signal input.

Let us now turn to the two-band (equal-width sub-bands) QMF-based converter. Because of the band-splitting operation, half of the input power \( \sigma_w^2 \) is delivered to each sub-converter. Thus, the maximum amplitude of the input signal to each sub-converter is now reduced and the new full-scale voltage is \( V_{fs} / \sqrt{2} \). As a consequence, the quantization noise power at the output of each sub-converters is \( \sigma_q^2 / 2 \). Each synthetic filter eliminates half of the quantization noise power (leaving the signal power intact), the quantization noise power at the output of each synthesis filter is \( \sigma_q^2 / 4 \). Since these sub-band noise signals are uncorrelated, the total noise power at the output of the system is \( \sigma_q^2 / 4 + \sigma_q^2 / 4 = \sigma_q^2 / 2 \). The total signal power, on the other hand, is \( \sigma_w^2 / 2 + \sigma_w^2 / 2 = \sigma_w^2 \). In other words, for a wideband input signal, the two-band QMF-based converter produces half of the quantization noise power that is produced by the time-interleaved A/D converter, which means a gain of 3 dB in the signal-to-noise ratio, i.e.
\[ SNR_{w}^q = 10 \log_{10} \frac{\sigma_w^2 / 2}{\sigma_q^2 / 2} = SNR_{w}^q + 10 \log_{10} 2. \]

This result can be generalized for the case of an array of \( M \) sub-converters as follows:
\[ SNR_{w}^q = SNR_{w}^q + 10 \log_{10} M, \]

corresponding to an increase in the number of effective bits given by
\[ \nu_{qur} = \log_{10} \sqrt{M}. \]

In summary, the use of bandpass filters before and after an array of \( M \) quantizers leads to an increase of \( \log_{10} \sqrt{M} \) effective bits of resolution, when digitizing a wideband signal.

In the cases in which the spectrum of the input analog signal has an energy distribution known a priori, lower resolution sub-converters can be assigned to those bands having lower energy. By appropriately allocating the bits in different bands, the quantization noise power can be separately controlled in each band, and the shape of the reconstruction error spectrum can be controlled as a function of frequency. This strategy,
known as sub-band coding has been used in many speech and image applications. A suitable bit allocation strategy allows for further reduction of the hardware complexity without introducing any degradation in the signal-to-noise ratio. This is illustrated next through simulation results obtained with images.

SIMULATION RESULTS

Due to the nature of most practical images, the so-called upper bands, containing the high spatial frequencies, are perceptually very important in some regions, but contribute only to a small percentage (e.g., 1%) of the total signal energy. As mentioned previously, one of the advantages of the QMF-based A/D converter scheme is that lower resolution subconverters can be assigned to the bands having smaller signal energy, resulting in further silicon area savings, and still retaining higher signal-to-noise ratio than the time-interleaved approach, even in the presence of mismatches among the subconverters. In this section we present simulation results obtained with image signals.

The model shown in Fig. 4 for the subconverters has been used in the simulations. The functional block Q \( f \) represents an ideal uniform quantizer, and \( e_{i,j} \) is the gain error associated with the \( k \)-th sub-convertor. The gain errors are obtained from the slope of the straight line that best fits, in the mean square error sense, the actual characteristics of the sub-converters. The "Lena" image shown in Fig. 5(a) (512 x 512 pixels, monochrome) has been used as the test image.

The image resulting from a time-interleaved array having four 6-bit sub-converters is shown in Fig. 5(b). The image is digitized by columns, so that the pixels of the \( f \)-th line are scaled by the factor \((1+e_{i,j})\), where \( e_{i,j} \) denotes "module 4". Since 512 is a multiple of 4, horizontal lines are generated. Diagonal lines are created when the number of sub-converters used to digitize the image is not a divisor of the total number of lines. For this image a signal-to-noise ratio \( SNR = 16.43 \) dB has been obtained, where the \( SNR \) is defined as

\[
SNR = 10 \log_{10} \frac{\sum u_{i,j}^2}{\sum (u_{i,j} - v_{i,j})^2},
\]

where \( u_{i,j} \) and \( v_{i,j} \) denote the original and processed pixels, respectively. Observe that this value of \( SNR \) takes into account the quantization noise (introduced by the ideal quantizers) and aliasing noise (due to mismatches among the sub-converters), according to the model of Fig. 4.

Next, a two-band QMF bank has been used for each of the image dimensions, so that again four sub-converters have been employed (the same sub-converters used in the simulations with the time-interleaved converter). The QMF bank is composed of linear phase FIR filters of length \( N = 8 \), whose coefficients can be found in [6, page 402]. Using a 6-bit sub-convertor in each of the four sub-bands (low-low, low-high, high-low, and high-high) of the image, a signal-to-noise ratio \( SNR = 32.02 \) dB is obtained, which is an improvement of 15.59 dB when compared to the time-interleaved approach. The resulting image is shown in Fig. 5(c). In order to exploit the energy distribution through the sub-bands, 6 bits have been allocated in the low-low sub-band, 3 bits in the high-high sub-band, and 2 bits in the low-high and high-low sub-bands. Figure 5(d) depicts the image obtained in this case. The corresponding signal-to-noise ratio is \( SNR = 24.77 \) dB, which is still 8.34 dB larger than that obtained with the time-interleaved method. In both cases, as Figs. 5(c) and 5(d) show, the effect of gain mismatches among the sub-converters is virtually eliminated by virtue of the analysis and synthesis filter banks. With the proposed method, therefore, it is possible to achieve better performance than the time-interleaved approach, with additional savings in die area. In such cases, however, a gain stage with high accuracy should precede the sub-converters having smaller resolution.

LIMITATIONS AND DESIGN CONSIDERATIONS OF THE SWITCHED-CAPACITOR ANALYSIS FILTER BANK

Finite Gain Error Reduction Technique

Despite the fast technological progress in the last twenty years, very accurate processing of high-frequency signals is still a difficult task. The speed limitation of analog switches and active elements are the main factors responsible for placing upper frequency limits to the processing of signals directly in the analog domain by either continuous-time or SC techniques. While analog switches can be made fast by a suitable dimensioning and driving, active elements can only be made fast at the cost of a low dc gain. The existing tradeoff between speed and gain makes it impossible to achieve high bandwidth and high gain simultaneously.

Precise switched-capacitor circuits always require the use of operational amplifiers. The clock frequency in sampled data systems must be larger than twice the signal bandwidth, and in order to avoid errors coming from the speed limitation, the clock frequency must be at least four times smaller than the gain-bandwidth product of the operational amplifier. As a consequence, for high-frequency input signals, the gain-bandwidth product of the operational amplifiers used in SC circuits must be very high, i.e. at least eight times larger than the signal bandwidth.

An operational amplifier can be made fast by increasing the bias current or, in order to reduce the non-dominant node capacitances, by reducing the transistor dimensions. However, in this case the output impedance of the transistor decreases and the dc gain is lowered. Several circuit techniques capable of reducing the finite gain effects of the operational amplifiers have been proposed in the literature. A novel circuit technique for the SC implementation of simple transfer functions with a reduced dependence on the finite gain of the operational amplifiers has been reported in [5], where single-stage operational amplifiers with moderate dc gain but very high bandwidth have been used.

Noise Generated by the Switched-Capacitor Filters

One of the most important aspects in a monolithic implementation of the QMF-based converters is the noise generated by the SC filters. The major difference existing between the QMF-based and the time-interleaved converters is that suitable bandpass filters are used, in the former case, before and after the quantizers. The quantization noise power as well as the noise introduced by the SC circuits, is spread over the Nyquist band, and because of the post-filtering action, only part of the noise power is transmitted to the output. Thus, only the power of the noise in the band of interest is collected, and no significant degradation of the S/N ratio results, as, by contrast, happens with a pure interleaved architecture. Let us then turn our attention to the noise generated by the SC circuit.

The predominant noise sources in SC filters are 1/f (low frequency) noise and thermal (wideband) noise [12]-[14]. The effects of 1/f noise are considerably reduced in our circuit design scheme, since there is a strong correlation between adjacent samples of this low frequency noise [15]. The white noise contributed by the operational amplifiers is low because of its...
high input pair transconductance used in high-frequency applications. Therefore, the main limitations are introduced by the thermal noise generated by the on-resistance of the MOS switches. The reason for this phenomenon is that the bandwidth of the thermal noise signal exceeds the sampling frequency by several orders, and, as a consequence, the sampled-data noise is highly undersampled resulting in the occurrence of an aliasing effect. The aliasing due to the sampling of the noise concentrates the noise power of the switch on-resistance into the baseband (the frequency range up to the Nyquist frequency). We, therefore, focus our discussion on the effect of the sampled-and-held noise only, which is generated by the switches.

To illustrate our discussion we consider the situation in Fig. 3(a). If we assume that \( V_m = 0 \), then during intervals of time when the switch is closed the equivalent circuit is that of Fig. 3(b), with \( R_m \) be the switch on-resistance. The noise voltage \( n_m \) is a broadband signal associated with \( R_m \). Thus, the noise waveform across the capacitor is the result of a broadband noise being filtered by an RC circuit.

When the switch opens the noise voltage is sampled and remains frozen in \( C \). Because this noise is not bandlimited to less than half the sample rate, the operation sampling causes the resulting noise power to be folded down to the baseband. The mean square value of the noise across \( C \) is then given by [16]

\[
\frac{\sigma^2}{C} = \frac{kT}{C},
\]

where \( k \) is the Boltzmann's constant and \( T \) is the absolute temperature. In other words, the aliasing due to the sampling of the noise concentrates the full noise power \( kT/C \) of the switch on-resistance into the baseband. In an SC filter this noise contribution is transmitted to the output with a given transfer function, which, to a first approximation, is here considered to be equal to 1.

In SC filter implementations with discrete components the value given by Eq. (11) is, in general, negligible. In monolithic implementations, however, \( \sigma^2 \) may assume high values. For switched-capacitors in the range of 0.25 – 0.5 pF, for instance, the value of \( kT/C \) are in the range of 0.006 – 0.016 (mV)\(^2\).

In order to access the limitations imposed by the noise generated by the SC filters, we compare it to the quantization noise produced by each sub-converters, given in Eq. (1). For \( V_{ref} = 1 \) V and \( k = 11 \) bits, we have \( \sigma^2 = 0.079 \) (mV)\(^2\). This result shows that if capacitors in the range of 0.25 – 0.5 pF are used, then the noise generated by the filters limit the resolution of the QMF-based converters to 10 – 11 bits, well beyond the usual specification for video applications.

CONCLUSIONS

Some theoretical and practical aspects, which are important for the monolithic implementation of QMF bank data converters have been considered. An estimate of the total noise power at the output of the converter due to the SC filter bank, has been obtained and then compared to the quantization noise power. Based on this study, we conclude that the noise generated by the SC filters has negligible contribution in most video applications. In those cases the quantization noise produced by the sub-converters has predominant effect.

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Figure 1 - Time-interleaved A/D converter.

Figure 3 - Model used for the sub-converters used in
the simulations.

Figure 2 - Analog-to-digital converter incorporating a
quadrature mirror filter bank.

Figure 4 - Model used to estimate the effects of sampled-
and held noise in the QMF-based converters.
Figure 5 - Simulation results: (a) Original image; (b) Image obtained with a time-interleaved converter. Notice the horizontal lines caused by mismatches among the sub-converters; (c) Image obtained with a QMF-based converter with 6 bits/band; (d) QMF-based converter having the following bit allocation: 6 bits (low-low band), 3 bits (low-high band), 3 bits (high-low band), and 2 bits (high-high band).