A HIGH FREQUENCY CMOS POWER BUFFER WITH EXTENDED LINEARITY

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ABSTRACT - A CMOS power buffer suitable for high frequency applications is discussed. The use of a high-speed push-pull output stage and a highly-linear common mode feedback allow good linearity to be maintained even with very high input frequencies. Indeed, Total Harmonic Distortions (THD) as good as -66 dB and -58 dB are achieved at 0.5 MHz and 1 MHz, respectively, with a load resistance of 75 Ω. Moreover, the circuit provides a dc gain of 62 dB and a gain-bandwidth product of 60 MHz. The integrated prototype, realized using a 1.2 µm CMOS process, occupies a silicon area of 280 mils².

I. INTRODUCTION
Power buffers are very useful in many analog integrated circuits, since they allow a direct link with the external world, without requiring any out-of-chip buffer [1] [2]. Particularly, high performance CMOS circuits such as high frequency filters, high conversion rate D/A converters, etc., find a larger field of application whenever they also include a power buffer as final stage. Indeed, high frequency filters and D/A converters, used as stand-alone circuits, generally have to drive loads or coaxial cables with a typical resistance of 50-75 Ω. An example of such an application is the D/A converter driving the RCT (Ray Cathodic Tube) in a digital video system. Here, a 75 Ω coaxial cable could be directly connected to the D/A converter output [3].

Power buffers must provide linearity and flat frequency response over all of the signal frequency range. When signal bandwidths of hundreds of kilohertz are treated those same requirements lead to gain-bandwidth products of a few tens of megahertz.

At the state of the art, power buffers driving resistances smaller than 100 Ω and providing more than 60 dB of linearity exhibit gain-bandwidth products which are smaller than 10 MHz. Therefore, they have a flat bandwidth of a few tens of kilohertz [4] [5].

In this paper a high frequency power buffer is presented which is capable of driving a load impedance of 75 Ω in parallel with 25 pF. The circuit provides a gain-bandwidth product of 60 MHz and a Total Harmonic Distortion (THD) of -58 dB when applying a 1 MHz 2 Vpp input signal. These results, which largely exceed the state of the art, were obtained thanks to the use of a high-speed class AB output stage and a highly linear common mode feedback circuit.

II. CIRCUIT DESCRIPTION
A schematic block diagram of the power buffer is shown in Fig. 1. A high-gain fully differential input stage drives a low-gain class AB output stage. A common mode feedback circuit, CMF, stabilizes the common mode output voltage of the input stage [6]. Resistance RL and capacitor CL represent the external output load. The strategy we adopted in designing CMF was that of improving linearity at the expense of some decrease in speed performance. In effect, the trade off for linearity is advantageous, since only non-linearities place a severe constraint on the minimum gain-bandwidth

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product of CMF circuits, while gain-bandwidth values as low as the signal bandwidth could be sufficient to save swing.

**Input stage and common mode circuit**

A complete schematic of the input stage including CMF is shown in Fig. 2. The input stage is a differential folded cascode amplifier that provides 62 dB of dc gain. It introduces a non-dominant pole at a frequency as high as 600 MHz. Feedforward capacitors $C_{C1}$ and $C_{C2}$ reduce the negative phase shift due to the second pole.

The common mode feedback circuit CMF is made up of two source followers M12, M13 and M18, M19, and a voltage-to-current converter composed of resistances $R_{CM1}$ and $R_{CM2}$ and a common-gate M14-M17. A reference current source, $I_{RC}$, flowing into the diode-connected transistors M20, M21 establishes the common mode reference voltage, $V_{CM}$. This voltage is applied to the gate terminal of M16. Since M13, M16 and M19 are matched transistors biased with the same current values, by appropriately sizing the current mirror M17, M9 (M17, M10) the output common mode voltage can be kept to $V_{CM}$.

The use of poly resistances in CMF allows a highly linear operation to be achieved. The value of these resistances have been set to 10 kΩ in order to preserve linearity while maintaining the gain-bandwidth product, $f_{TCM}$, of CMF to around 10 MHz. This value is lower than that of the main amplifier, but, as mentioned before, it meets our target to enhance the linearity. The value of $f_{TCM}$ depends on resistances $R_{CM1}$, $R_{CM2}$ and capacitors $C_{C3}$ and $C_{C4}$ (see Fig. 3). It is given by

$$f_{TCM} = \frac{2}{2\pi R_{CM} C_C \alpha}$$  \hspace{1cm} (1)

where $C_C = C_{C3} = C_{C4}$, $R_{CM} = R_{CM1} = R_{CM2}$ and $\alpha$ is the gain of the inverter stage to which Miller capacitors $C_{C3}$ and $C_{C4}$ are applied.

**Output stage**

A schematic diagram of the output stage is shown in Fig. 3. It is formed by two low-gain inverting amplifiers M22-M24 and M25-M27, which are operated in a push-pull configuration, and a driving branch M28, M29. The differential input signal coming from the input stage is applied to the gates of M23 and M26. It produces complementary current signals in the diode-connected transistors M22 and M27 which are mirrored in the output transistors M28 and M29, respectively. In order to achieve an acceptable trade-off between speed and power consumption the mirror ratio between M22, M28 and M27, M29 was set to 6.

Capacitors $C_{C3}$ and $C_{C4}$ provide a Miller compensation, while $R_{C1}$ and $R_{C2}$ compensates for the right half-plane zero. The frequency response of the output stage is the following

$$H(j\omega) = 2 \alpha \frac{1 + j\omega \frac{C_{gs23}}{g_{m23}}}{1 + j\omega \frac{C_{gs23} + C_{PB}}{g_{m24} + g_{m23}}} \frac{1}{1 + j\omega \frac{C_{PA}}{G}} \frac{1}{1 + j\omega R_C C_L}$$  \hspace{1cm} (2)

where

$$\alpha = \frac{g_{m23} g_{m24}}{g_{m22} (g_{m23} + g_{m24})}$$

$$G = g_{m22} + \frac{g_{m23} g_{m24}}{g_{m23} + g_{m24}}$$

and $C_{PA}$, $C_{PB}$ are the parasitic capacitances at nodes A (or A') and B (or B'), respectively. Since the values of $g_{m23}$ and $C_{gs23}$ are greater than that of $g_{m24}$ and $C_{gs24}$, respectively, the first term in eq. 2 is nearly equal to one for any frequency. The pole due to
node A (A') (second term) has been moved from its value \( \frac{g_{m22}}{2\pi C_{PA}} \) before compensation, to a high frequency \( \frac{G}{2\pi C_{PA}} \) after compensation. It gives a negligible phase contribution to the phase shift. The last term accounts for the pole due to the load impedance.

Typically, Miller capacitors are connected to the output node thus placing a limit on the maximum value of load capacitance. In our case, the compensation capacitors are connected to internal nodes of the output stage, as a result load resistances and capacitances will together determine the second pole. Therefore, in order to preserve stability, the output pole, \( f_{out} \), and the gain-bandwidth product, \( f_{gbw} \), have to meet the following condition

\[ f_{out} \leq f_{gbw} \]

This, however, is not a severe limitation to the use of the circuit since load resistances usually employed in high frequency applications are as low as 75 \( \Omega \) or 50 \( \Omega \). Assuming such resistance values, load capacitances from 35 pF to 50 pF can be driven, without incurring in stability problems.

III. EXPERIMENTAL RESULTS

The circuit was fabricated using a 1.2 \( \mu \)m CMOS process. A die photo is shown in Fig. 4. The area of the core is 280 mils\(^2\). Experimental measurements were carried out with an output impedance of 75 \( \Omega \) in parallel to 25 pF. Fig. 5 shows the frequency response. The measured dc gain and the gain-bandwidth product are 62 dB and 60 MHz, respectively. A linearity measurement in a buffer configuration with an input signal of 2 Vpp and 1 MHz of frequency is shown in Fig. 6. The second and third harmonics are 64 dB and 60 dB lower than the fundamental frequency, respectively. The amplifier can be used, of course, with different resistive feedbacks. In these cases, the linearity reduction caused by the loop-gain reduction is partially compensated, since only small common mode input signals have to be rejected.

The curve in Fig. 7 depicts the second and third harmonics versus frequency. Compared with previously reported implementations [4] [5], this circuit achieves the same linearity at a frequency five or more times higher, while driving the same output resistance. Moreover, in spite of a relatively high power consumption, the gain-bandwidth to power consumption ratio is higher than in previous designs.

Some of the main electrical features of the buffer are summarized in Table I.

CONCLUSION

A power buffer has been presented which can be used with high performance analog circuits such as high frequency filters and D/A converters. Experimental measurements show that more than 60 dB of linearity is maintained for signal frequencies of several hundreds of kilohertz. Furthermore, the high gain-bandwidth value allows a flat frequency response to input frequencies greater than 1 MHz.

ACKNOWLEDGEMENT

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REFERENCES


Fig. 1. Block diagram of the buffer.

Fig. 2. Schematic diagram of the input stage and CMF.

Fig. 3. Schematic of the output stage.

Fig. 4. Die photo.

Fig. 5. Amplitude of the frequency response.

Fig. 6. Power spectrum for a 2 V pp 1 MHz input signal.

Fig. 7. Harmonics versus frequency for a 2 V pp input signal.

**TABLE I**

Typical measured performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>Open-Loop Gain</td>
<td>52 dB</td>
</tr>
<tr>
<td>Gain-Bandwidth Product</td>
<td>60 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>56°</td>
</tr>
<tr>
<td>Settling Time (1 V, 0.1%)</td>
<td>50 ns</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>155 V/μs</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>40 mW</td>
</tr>
<tr>
<td>Chip Size</td>
<td>280 mm²</td>
</tr>
<tr>
<td>THD (Vin = 2 Vpp, 75Ω/25 pF)</td>
<td></td>
</tr>
<tr>
<td>20 kHz</td>
<td>-72 dB</td>
</tr>
<tr>
<td>1 MHz</td>
<td>-56 dB</td>
</tr>
<tr>
<td>PSRR 1 kHz</td>
<td>60 dB</td>
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<tr>
<td>PSRR 1 MHz</td>
<td>50 dB</td>
</tr>
<tr>
<td>CMRR 1 kHz</td>
<td>70 dB</td>
</tr>
<tr>
<td>CMRR 1 MHz</td>
<td>54 dB</td>
</tr>
<tr>
<td>White Noise</td>
<td>20 nV/√Hz</td>
</tr>
<tr>
<td>Picon Noise (1 kHz)</td>
<td>125 nV/√Hz</td>
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