AN OFFSET-COMPENSATED CONTINUOUS-FEEDBACK SC INTEGRATOR FOR BIQUAD SECTIONS

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ABSTRACT

An offset-compensated SC integrator is presented, which is stabilized via a continuous feedback and where the slewing of the output voltage is eliminated, or at least limited, with respect to other offset-insensitive circuits. The integrator is suitable to be inserted into general biquadratic sections, where the offset of the operational amplifier does not influence the output, moreover, a continuous time voltage is supplied at the output node. Simulated responses of one biquadratic filter are given and show that the offsets as well as the equivalent 1/f noise generators of both the operational amplifiers are fully filtered at the output node. 

Introduction.

Biquad filters are basic building blocks for the synthesis of high order sections, either for cascaded, or for multiple loop feedback, or coupled biquad topologies. Several universal SC biquad circuits have been proposed in the literature[1], [2], [3], and are extensively used for high precision applications. A further significant requirement for such a section could be an inherent insensitivity to the offset of the operational amplifiers as well as to their low-frequency noise sources. Such a result is obtainable by using time-sharing technique [4], if both the integrators in the biquad are resistively damped (dual-terminated second order SC active ladders), or by a proper use of only one offset-insensitive integrator [5], to get an offset-insensitive biquad structure [6].

The main characteristic of the circuit proposed in [6] is that the output voltage is time-continuous and no Sample & Hold is required with respect to similar circuits [7]. However, the operational amplifier of the other integrator is continuously set in the buffer connection during one half of each clock period. This fact implies some instants of open loop situation and a slewing of the output voltage that can be as large as the allowable output swing. This situation is common to other noise-cancelling SC filtering techniques [8].

The present communication wishes to consider the feasibility to remove such further limitations, to get offset-compensated switched-capacitor biquads in which the operational amplifier less suffers of slewing limitations and is stabilized via a continuous feedback, avoiding any possible latch-up.

The offset compensated continuous-feedback integrator.

In Fig. 1 the offset-compensated integrator, with a continuous feedback and no slewing limitation, is given. The circuit is clocked by two non-overlapping phases, 1 and 2. \( X_0 \) represents the input referred voltage generator which models both the low-frequency error sources of the operational amplifier, i.e. the dc-offset and the 1/f noise contribution. For obtaining the sampled data transfer function \( \frac{V_o}{V_i} \), we assume \( X_E = 0 \), there results that capacitors \( C_X \) and capacitor \( C_P \) are inactive for the signal amplification. The integrating capacitor value is set by the parallel \( C_A + C_A \), and the transfer function.

![Fig. 1 Offset-compensated continuous-feedback SC non-inverting integrator](image-url)
with the output voltage seen during phase 2 is given by

\[
\frac{V_2}{V_{o2}} = \frac{C_1}{C_2 + C_p} \frac{v}{z - 1}
\]  

(1)

The inverting integrator is obtained by using for \(C_1\) a non-inverting blocking scheme, while the transfer function becomes

\[
\frac{V_o}{V_{in}} = -\frac{C_1}{C_2 + C_p} \frac{v}{z - 1}
\]  

(2)

The capacitor \(C_2\) i.e any fraction of the inverting capacitance \(C_2 + C_p\) is always in feedback connection and at any instant ensures the operational amplifier a stable differentiating function.

Capacitors \(C_2\) are for compensating the errors due to the offset \(X_0\) during phase 1; they are in parallel and are charged at \(X_0\) through \(C_p\) and \(C_2\) rather than through a buffer connection of the operational amplifier as used in other circuits [9, 17, 18]. During phase 2, capacitors \(C_2\) are in series and if

\[
C_A = 2 \frac{C_1C_2 + C_pC_2 + C_2C_p}{C_p + C_2}
\]  

(3)

they supply exactly the same amount of charge required by \(C_2\) to be charged at \(X_0\) and by \(C_p\) to be discharged of the charge due to \(X_0\) and collected at it during phase 1, so no charge due to \(X_0\) will be delivered to the parallel \(C_2 + C_p\) and the output \(V_o\) during phase 2 is then free of errors due to the operational amplifier.

Capacitor \(C_A\) is switched between ground and virtual ground, while it remains always connected to the output node; this ensures a limited voltage step in the output voltage from phase 1 to phase 2, when the offset \(X_0\) is non zero, otherwise the output voltage does not change in the two half cycles period.

For having a small value of \(C_p\) capacitors we need to set \(C_2\) as low as possible, while the voltage step at the output node will be as lower as possible in the capacitor \(C_A\).

Minimum switch forms are also possible in this case, as the offset-compensated integrator of Fig. 2 can further be modified for the cases of Figs. 12 and 13, where it verified that under the condition \(\alpha = 1 + X_0\) the circuit of Fig. 2 works as an active integrator with the integrating capacitance value given by \(C_2 + C_p\). The condition on \(C_2\) capacitors to get the wanted filtering action on its low frequency error factor \(X_o\) is now given by

\[
X_0 = \frac{C_2C_p}{C_p + C_2}
\]  

Moreover, eq. (4) shows that a smaller value of \(C_p\) is required with respect to the first circuit in fact, \(C_p\) is in parallel connection with the virtual ground and its operation is then free of errors due to \(X_0\).

In the circuit of Fig. 2 the output voltage step due to incoming signals will result twice larger than in the circuit of Fig. 1.

Offset insensitive biquads

The circuit of Fig. 1, as well as its inverting counterpart, can be used in anyone of the known two-op-amp biquad structures [1, 2, 13] in place of the non-damped integrator if a resistive damping is used, or as the input-integrator if a capacitive damping is used. In this latter case the damping capacitor must be disconnected during the precharging of \(C_p\) capacitors.

It is worth noting that the offset of the second amplifier in anyone of the two-op-amp biquads considered in [1, 2, 13] does not influence at all the output voltage being the first integrator not damped in fact, its input SC structure placed in the loop will not deliver to it any charge, which implies that the output of the other op-amp must be zero regardless of its equivalent input referred voltage generator [16].

Fig. 3 shows the resulting circuit when the modified inverting integrator is used in the biquad proposed in [2]; the transfer function of the circuit holds

\[
\text{Fig. 2 Modified offset-compensated continuous-feedback SC integrator for a minimum switch form}
\]
Fig. 3: SC biquadratic block due to MARTIN and SEDRA [2] including the modified integrator.

Fig. 4: SC biquadratic block due to LIN and TSENG [3] using the modified integrator.

\[ H_i(z) = \frac{K_e z^2 + (K_1 K_2 - 2 K_3) z + (1 - K_9 K_6)}{z^2 + (K_4 K_5 + K_8 K_6 - 2) z + 1} \]

which is exactly the same transfer function of the original circuit, in this case \( C_1 \) in eq (3) corresponds to \( (K_2 + K_4) C_1 \).

The modified integrator can be also used into the SC biquad proposed in [3], without modifying the original transfer function. The circuit is given in Fig. 4, while the transfer function is

\[ H(z) = \frac{C_6}{C_4 + C_8} \]

\[ z^2 z^2 + \left( \frac{C_6}{C_0} - \frac{C_1}{C_2} \right) z + \frac{1}{C_0} \]

\[ z^2 z^2 + \left( \frac{C_6}{C_4} - \frac{C_1}{C_4} \right) z + \frac{1}{C_4} \]

The value for \( C_1 \) to be used in eq. (3) is given by \( C_1 + C_7 \).

The use of the modified integrator in the E-type and F-type SC biquads proposed in [1] requires to modify the clocking scheme of the switches. Among the possible new switch arrangement we have choose to invert only the phasing of the switched capacitor \( A \) as shown in Fig. 5; this leads to a minor difference in the transfer function with respect to the original ones, since if the output is observed during phase 2, the original transfer functions hold, respectively, given for the E and F circuits as

\[ H_E(z) = \frac{z^2 + (G - i - j) z + (i - H)}{z^2 + (C + F - 2) z + 1} \]  
\[ H_F(z) = \frac{z^2 + (G - i - j) z + (i - H)}{(F + 1) z^2 + (C - F - 2) z + 1} \]

To get eqs (7) we put \( A = B = D = 1 \). The value to be used for \( C_1 \) in eq. (3) is in both E and F cases given as \( C + G + H \).
We always assume that the voltages are sampled and held over a full clock period, but this is not a necessary constraint; the modifications that results are similar to those due for the original cases.

An example

The circuit of Fig. 3 was designed for a low-pass notch response, with $f_N = 1.7KHz$ and $Q = 30$, being the clock frequency set at $128KHz$, for that we have $K_v = 0$.

Fig. 7 shows the Diana [9] simulated amplitudes of the response of the filter $|H(e^{j\omega})|$ and of the responses to the output of the filter from the non-inverting input of each operational amplifier, say $|H_1(e^{j\omega})|$ and $|H_2(e^{j\omega})|$, respectively. A correlated-double-sampling filtering operation on the equivalent error sources of each operational amplifier results: this action is active against low-frequency contributions, hence, against offset and low-frequency components of the input referred noise generator of both the operational amplifiers.

REFERENCES


