SELF-CALIBRATION IN HIGH SPEED CURRENT STEERING CMOS D/A CONVERTERS

S Boiocchi*, S Brigati*, G Caiulo**, F Maloberti*

*University of Pavia, Italy; ** Italtel Srl, Italy

ABSTRACT

This paper describes a novel approach to self-calibration applied to current steering CMOS DACs. The basic idea is to use regulated cascode current sources with degenerated resistances. The drop voltage across the degenerated resistance measures the current, thereby allowing calibration. A suitable architecture for achieving continuous calibration is described. The paper also discusses some design problems and proposes a new differential switch current cell which alleviates the glitches deriving from the clock feedthrough effect.

1 INTRODUCTION

Video D/A converter architectures can be classified into two general categories: voltage switching and current switching converters.

The first class includes converters based on resistive and/or capacitive selection networks which can be intrinsically monotonic and can also determine high integral and differential linearity. Moreover, power consumption is generally lower than in current switching solutions. However, a high number of analog switches is needed for the selection function. This constitutes an intrinsic limitation to the maximum achievable speed (Pelgrum (1)).

The second category includes, in particular, DACs based on the current cell matrix principle which generally reach the highest conversion rates (Miki et al (2), Takakura et al (3)). A resistive load receives a variable number of elementary currents (depending on the input code) to produce the analog output voltage. This kind of D/A converter allows fast and accurate settling if switches are driven simultaneously and if their charge injection (clock feedthrough) is suitably controlled. However, the use of small size transistors increases the mismatch between current sources. This, in turn, degrades differential linearity and monotonicity. The problem can be overcome by the use of self-calibration techniques already proposed for low frequency applications. To implement self-calibration we need a specific calibration phase, for example, at start-up. In this case, however, we do not take into account parameter variations due to short term modifications in operating conditions. On the contrary, they are accounted for by continuous-time calibration (Huijsing et al (4)).

This communication presents a possible solution for the implementation of a continuous-time self-calibration in a 10-bit CMOS D/A converter.

2 DESIGN CONSIDERATIONS

This section discusses some of the most important design issues for high speed CMOS current steering D/A converters.

The worst limitation of such a category of converters comes from the current sources mismatch that limits the resolution to below 8 bits. This source of error can be compensated at the first order by suitable switching strategies and with a common centroid arrangement of current sources. With careful layout 10-bit accuracy can be achieved (2, 3). However, since the result relies on well controlled second order non-linearities, we believe that the use of a self-calibration technique corresponds to a more solid guarantee. We will discuss the proposed implementation for this solution in the following section.

A second important design issue concerns the fast switching of elementary current sources. Fig. 1 shows what is commonly used: a heavily imbalanced differential pair injects the cell current into one or the other of the two terminations depending on the control signals $\Phi_{ON}$ and $\Phi_{OFF}$. This structure leads to fast switching and fast settling. In fact, the cell does not have high impedance nodes which could limit time constants. However, a restriction to settling comes from charge injection (Shien et al (5)).

![Figure 1: Standard current cell](image)

With the switching, either towards the real load or to the dummy load, we have an injection of charge whose sign contrasts the desired transition of the output signal. This produces a clock-feedthrough glitch as shown in Fig. 2. We overcome the above limit by using the topology shown in Fig. 3: n-channel transistors replace the p-channel switches. The charge injection associated to the clock-feedthrough helps the transition of the output signal and immediately charges the parasitic capacitances towards their final value. Assuming $M_1$ to be switched on, the steady state output voltage will increase by

$$V_{LSB} = I_{LSB} R_L$$  \hspace{1cm} (1)

where $R_L$ is the output resistive load. We note that an amount of charge equal to $Q_L = C_L V_{LSB}$ is needed. With a proper sizing of the switches we can provide this amount of charge from the channel injection itself. Assuming very fast transitions the channel charge is equally split between source and drain and a net amount of charge (positive or negative depending on the transition) equal to half the channel charge is injected into the load. This leads to the following design condition:

$$Q_L = \frac{1}{2} q_{ch} = \frac{1}{2} C_{ch} W L (V_{GS} - V_{th})$$  \hspace{1cm} (2)

Fig. 4 shows the simulation results for the new cell. We observe that a suitable switch sizing allows us to practically cancel the glitch.

3 SELF CALIBRATION IN THE BASIC CELL

We achieve the calibration of a generic current cell with a common calibration block (made by $R_{ref}$, $R_{cal}$ and the op-amp in Fig. 5).

The current of the generic $i$-th cell depends on the $V_{GS}$ of a saturated transistor $M_i$ degenerated by the resistor $R_i$. During the calibration phase the switches $SW_3$ and $SW_2$ are on while $SW_3$ is turned off. $R_{cal}$ (nominally equal to $R_0$) takes over the role of the degenerated resistance and the feedback loop makes the voltage drops across $R_{ref}$ and $R_{cal}$ equal by setting the voltage across the gate to source of $M_1$ to a suitable value. This voltage is also stored on capacitor $C_1$ to allow the cell to operate normally.

With the solution used any mismatches and limits in the calibration block (op-amp finite gain, differences between $R_{ref}$ and $R_{cal}$) are reflected only in a gain error that will be the same for all the calibrated cells. Therefore, we can globally adjust this error by slightly changing $I_{ref}$.

Moreover, we observe that conversion accuracy is limited by the relatively low output impedance of the elementary current source. Fig. 6 shows the equivalent circuit of the converter output section, when $n$ current sources are activated for conversion. Each of the current sources is characterised by a current $I_{LSB}$ and a finite output resistance $r_{out}$. The analog output voltage becomes:

$$V_{out}(n) = I_{LSB} \frac{n R_L}{n R_L + r_{out}}$$  \hspace{1cm} (3)
If we compare equation (3) with the ideal characteristic of the converter (obtained assuming infinite $r_{out}$), we note that a finite value for $r_{out}$ produces an integral linearity error in addition to a gain error. This effect is not noticeable at medium resolutions. However, it has an influence when 10 bits of accuracy are required. To keep the linearity error below 0.5 LSB, the output resistance of the elementary current source should be at least 500 thousand times $R_L$. Assuming $R_L$ equal to 50 $\Omega$, $r_{out}$ would become too high to be realized by a simple MOS transistor.

The output impedance of the elementary current cell can be increased by the use of a regulated cascode current source, as proposed by Tsumazou et al (6) and Soin et al (7). The circuit in Fig. 7 still allows calibration while the output impedance of the current cell increases by the bootstrap amplification factor

$$A_{boo} = \frac{I_{mci}}{r_{sci}} \times \frac{I_{mas}}{r_{sas}}$$

The major problem, now, comes from the clock feedthrough injection over the storing capacitor $C_i$. We alleviate this problem with dummy elements and by using a suitable large value for $C_i$ (in our circuit we chose $C_i = 4$ pF).

A final possible limit could come from the leakage current of opened switches. A small current determines
Fig. 8 shows the calibration transition for correcting an exaggerated error. We note that the current reaches the correct value in less than 2 μsec and that the residual clock-feedthrough produces a lower than 0.1 % error on the calibrated current.

4 CONVERTER ARCHITECTURE

In the previous section we have seen how to achieve the calibration of a single current source. Here we describe the proposed architecture of a 10-bit DAC capable of achieving continuous calibration. A block diagram of the converter is shown in Fig. 9.

The circuit is made up of 32 MSB current sources (each characterised by a current $I_{\text{MSB}} = 32 I_{\text{LSB}}$) and two banks each with 32 LSB current sources. Calibration is continuously performed during the normal operation of the converter using the following strategy: we periodically submit to calibration one of the MSB current sources or one of the two LSB banks. Therefore, a complete calibration cycle is made up of 33 elementary calibration periods. The calibration sequence used is shown in Fig. 10. The MSB cells are numbered from 0 to 31 and the two LSB banks are called $\mathbf{f}$ and $\overline{\mathbf{f}}$.

For the normal operation of the converter we always have 31 MSB cells available together with at least one of the two LSB banks. The problem now is the management of the 31 MSB cells. This is achieved using a proper control logic. A counter generates the
index $K$ of the MSB cell currently under calibration. This counter is locked when one of the two LSB banks is under calibration.

The cell whose index is $K + 1$ plays the role of the first cell to be switched on for conversion. The 5 MSBs of the input word are then added to the index $K$ and the result defines the last cell to be switched on.

We designed a specific logic (MSB Selection Logic plus Calibration Logic given in Fig. 9) for a simultaneous selection of the cell to be calibrated and the ones used for conversion. The circuits used minimise the number of cascaded gates and consequently the total gate delay. The simulation results show that by using conventional 1.2 $\mu$m CMOS technology we can achieve a speed of up to 100 MHz in the logic section.

The LSB bank to be calibrated is selected by using a toggle flip-flop controlled by the calibration command of the 31st MSB cell. Since we perform a global calibration of the LSB bank, to minimise errors we use a common centroid strategy in selecting LSB current sources (3).

5 CONCLUSIONS

This paper has presented a 10-bit DAC based on a current switching architecture for video applications. The use of a continuous-time calibration stage together with a new current cell topology allows the converter to be run with a clock signal frequency of up to 100 MHz.

6 ACKNOWLEDGEMENT

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7 REFERENCES