Design of Analog Blocks for Low-Voltage Switched Systems

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ABSTRACT
Design of low-voltage CMOS analog circuits becomes particularly critical when switches are involved. To drive them into the on-state a gate voltage which is higher (or lower) than the handled signal by at least the threshold voltage is required. This strongly reduces the signal swing allowed. To overcome this problem a novel approach, the “switched” operational amplifier, has recently been proposed. The idea is very interesting but it suffers from a number of practical problems. In this paper we discuss existing solutions and we suggest a new implementation. Moreover, we propose a new approach, the “switched” unity gain amplifier and we discuss the implementation of switched capacitor building blocks with this solution. Finally, we present simulation results for the proposed circuits and provide some design guidelines.

INTRODUCTION
Technological evolution and market requirements are pushing towards low voltage and low power integrated circuits. This need comes from technology shrink (which lowers the breakdown voltage of the devices) and from the increasing demand for portable (battery operated) systems. The most critical limitation of CMOS technologies in low-voltage design is the relatively high threshold voltage ($V_{th} \approx 0.7$ V). Unfortunately, $V_{th}$ can not be reduced much while maintaining acceptable the leakage current of the transistors. Therefore, low-voltage operation in CMOS technology must be achieved using design techniques. In digital circuits we can use a supply voltage which is slightly higher than the thresholds, thus losing part of the noise margin. However, in analog circuits, especially when switches are involved, new solutions should be invented.

Two typical situations where low-voltage design is challenging are shown in Fig. 1: a sample and hold and a dumped switched capacitor (SC) integrator. The main problems that we have to face in the design of such circuits are the following: a) we should achieve a suitably wide input common mode range in the operational amplifier (OP-AMP) used in the sample and hold, b) we need a proper low (or high) input common mode range in the dumped integrator to allow a low (or high) value of $V^*$, c) we must ensure that all the switches can reach the on state under any operating conditions.

![Switched capacitor building blocks: sample and hold, dumped integrator](image)

Fig. 1 - Switched capacitor building blocks: sample and hold, dumped integrator

Recently new solutions for the above mentioned problems have been proposed [1] [2]. They are based on the “switched” operational amplifier principle. In this paper we will discuss the limits to these solutions, we will consider possible improvements and finally we will propose a novel approach based on a “switched” unity gain amplifier.

SWITCHED OPERATIONAL AMPLIFIER
The major limitation in low-voltage SC systems comes from the switches. The voltage that we have to apply to the gate in order to achieve the on state must be higher (or lower) than the channel voltage by more than $V_{th}$. If the switch is connected to a node whose voltage lies in-between the power supplies (for example the analog ground, $V_{AG}$, or the OP-AMP output node), this condition may not be satisfied. However, if we look at the schematic of the dumped integrator in Fig. 1 we see that this problem concerns only part of the switches, because some of them are (or can be) connected to voltages close to $V_{SS}$ or $V_{DG}$ (for example $V^*$) ensuring a satisfactory on-state, even without voltage elevators on board.

The idea behind the switched operational amplifier is to embed into the OP-AMP the critical switches connected to its output (for example $S_1$ or $S_2$). These switches open or close the connection between the output of the OP-AMP and the rest of the circuit. Therefore, to eliminate them while performing the same operation, we have to interrupt the signal path inside the OP-AMP and force its output to a high
impedance state.

OP-AMPS used in SC applications are usually transconductors (OTA) whose typical output stage is shown in Fig. 2a. In this case it is possible to interrupt the signal path by switching off the two current sources, $M_1$ and $M_2$, acting on the top and the bottom as shown in Fig. 2b. When the two transistors $M_{SW1}$ and $M_{SW2}$ are turned off the output of the OP-AMP is in the high impedance state, as required.

![Fig. 2 - Output stages: (a) conventional OP-AMP, (b) switched OP-AMP](image)

In order to further reduce it, therefore, we need to eliminate $C_C$.

![Fig. 4 - Simulated voltage across capacitor $C_I$ during the on-off transition of the two-stage switched OP-AMP](image)

This was proposed in [1] using a two-stage OTA, as shown in Fig. 3. If we analyze this solution we encounter two drawbacks: asymmetric switching times of the two current sources, $M_1$ and $M_2$, from the on to off state may cause undesirable current injection into capacitor $C_I$. Moreover, because of the circuit topology, the switching times of $M_6$ and $M_7$ are also asymmetric. Therefore, we have an additional injection of current into $C_I$ through the compensation capacitor ($C_C$).

In fact, the current in $M_1$ is interrupted immediately after the clock edge, while the current in $M_2$ and $M_7$ flows until their gate capacitances are discharged through the on resistance of $M_{SW1}$. Likewise, $M_5$ is switched off directly by $M_3$, while $M_7$ has a delay due to the time constant of the current mirror $M_6$-$M_7$.

These drawbacks can be reduced by opening $S_3$ (or $S_4$, depending on the configuration) before switching off the OP-AMP. However, a residual effect due to parasitic capacitance $C_P$ is unavoidable. Fig. 4 shows a simulation of the voltage across $C_I$ during the on-off transition. Although $S_3$ was switched off before the OP-AMP, and in spite of the small bias current ($500 \text{ nA}$), we observe a residual error of about $4 \text{ mV}$, which is unacceptable for many applications. This error is mainly due to the effect of the compensation capacitor. In order to further reduce it, therefore, we need to eliminate $C_C$.

![Fig. 5 - Single-stage switched OP-AMP](image)

### Table 1 - Simulated performances of the single-stage switched OP-AMP

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>$&gt; 64 \text{ dB}$</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>$80^\circ$</td>
</tr>
<tr>
<td>GBW ($C_I=2 \text{ pF}$)</td>
<td>$500 \text{ kHz}$</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>$0.2 \text{ V/\mu s}$</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>$7.5 \mu \text{W}$</td>
</tr>
<tr>
<td>Power Supply</td>
<td>$1.5 \text{ V}$</td>
</tr>
<tr>
<td>Output Swing</td>
<td>$1 \text{ V}$</td>
</tr>
</tbody>
</table>

A possible solution is shown in Fig. 5. It is a single-stage OP-AMP, which does not need an internal compensation capacitance, thus avoiding the above mentioned problems. A suitable DC gain is ensured by using a cascode topology in the output stage. In particular, in order to obtain the best trade-off between output voltage swing and gain, high-
compliance cascode mirrors were used [3]. Using this topology with a 1.5 V supply voltage, we can achieve a DC gain of more than 64 dB with an output voltage swing of about 1 V. Note that this value is only some tens of millivolts lower than in a conventional two-stage OP-AMP. The switching function is realized by transistors $M_{SW1}$, $M_{SW2}$ and $M_{SW3}$. The simulated performances of the proposed low-voltage switched operational amplifier are summarized in Table 1.

THE PROBLEM OF $S_2$

The approach discussed in the previous section does not provide a solution for all the critical switches in the dumped SC integrator in Fig. 1. Switches $S_2$ and $S_8$ cannot be implemented using a switched operational amplifier. In [2] a solution to this problem is proposed. It is shown in Fig. 6.

**Fig. 6 - Low-voltage switched capacitor integrator**

In order to guarantee a satisfactory on state for $S_2$, we have to switch node $V_I$ to $V_{SS}$ instead of the analog ground ($V_{AG}$). Therefore, an extra charge is injected into the summing node of amplifier $A_2$, introducing an equivalent offset. However, in the proposed solution, capacitor $C_{DC}$ injects the same amount of charge with the opposite sign, compensating this effect.

Consequently, $S_2$ is now connected to $V_{SS}$ so it can be switched properly (using an n-channel transistor). Moreover, since the additional SC branch, $C_{DC}$, is switched between $V_{SS}$ and $V_{DD}$, it is not critical (assuming that $S_{DC1}$ is a p-channel transistor).

In the described solution the value of the analog ground voltage is defined by a SC divider ($C_{DC}$–$C_I$). Unfortunately, the divider is parasitic sensitive and the result of the partition depends on $V_{DD}$. Therefore, any noise affecting the supply voltage will correspond to noise in the equivalent analog ground.

THE SWITCHED UNITY GAIN AMPLIFIER

The novel solution that we propose to implement critical switches in low-voltage SC systems is shown in Fig. 7. In this case the switching function is associated to unity gain buffers ($B_1$, $B_2$ and $B_3$).

These devices behave like normal buffers when the clock signal is high but they act as open circuits (i.e. the output is in a high impedance state, as in the switched operational amplifier) when the clock signal is low.

Ideally switched unity gain amplifiers could be used directly to implement switches. Unfortunately, in reality they are affected by non-linearity, especially when rail to rail voltage swing is required. The solution to this problem is shown in Fig. 7: we introduced buffer $B_4$ in the feedback loop, node X is the output of the integrator while node Y is connected to the next stage. If the two buffers $B_1$ and $B_3$ have the same transfer function, the voltage at node Y is a replica of the voltage at node X, in spite of non-linearities and finite gain.

**Fig. 7 - Low-voltage switched capacitor integrator implemented using switched unity gain amplifiers**

Using the proposed approach we can easily implement also switch $S_2$. In fact, when $B_2$ is in high impedance state we can connect node $Y$ to the required voltage, $V_{AG}$ by using the switched buffer $B_3$. Of course, the voltage at node $Y$ is not an exact replica of $V_{AG}$ because of the non-linear response of the buffer. Nevertheless, this is not a relevant problem since it corresponds to an offset. The dumped integrator of Fig. 1, implemented with switched unity gain amplifier is shown in Fig. 8.

**Fig. 8 - Low-voltage dumped switched capacitor integrator implemented with unity gain amplifiers**

Buffer $B_4$, as well as OP-AMP $A_2$ can be switched off (with a slight delay with respect to $B_2$) to reduce power consumption. The proposed solution can easily be made fully differential.

**Fig. 9 - Low-voltage sample and hold implemented using switched unity gain amplifiers**

The sample and hold is another critical block in low-voltage applications. In this case, too, the switched unity gain amplifier can be used to solve the problem. Let us consider
the block diagram in Fig. 9: during the first clock phase the input signal \( V_{in} \) is replicated at node \( Y \) by buffer \( B_1 \) (with a non-linear transfer function) and stored on capacitor \( C_S \). Then, during the other clock phase, \( C_S \) is connected in feedback around the OP-AMP through buffer \( B_2 \). Assuming that the two buffers \( B_1 \) and \( B_2 \) have the same non-linear response, the voltage at node \( V_{out} \) is a precise replica of the input signal.

**DESIGN OF SWITCHED UNITY GAIN AMPLIFIERS**

Large common mode swing is the only critical requirement for a switched unity gain buffer. Fig. 10 shows a possible solution.

![Proposed switched unity gain amplifier](image)

*Fig. 10 - Proposed switched unity gain amplifier*

In order to verify the performances of the proposed architecture, we simulated the circuit in Fig. 7 (short-circuiting capacitor \( C_2 \)), using the proposed switched unity gain amplifier. Fig. 11 shows the obtained non-linearity error in the DC transfer characteristics from the input to nodes \( Z \) and \( X \). It can be observed that the error at node \( Z \) is already very small, and it almost disappears at node \( X \), confirming theoretical predictions.

![Simulated output signal of the low voltage sample and hold](image)

*Fig. 12 - Simulated output signal of the low voltage sample and hold*

**CONCLUSIONS**

In this paper we analyzed existing solutions and open problems concerning the design of low-voltage switched systems. Moreover, we proposed a new approach based on switched unity gain amplifiers, which seems to be the definitive solution for many applications. Finally, a practical implementation of the switched unity gain amplifier, showing excellent performances, was presented.

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**REFERENCES**

