Switched Capacitor Dual-Collector Magnetotransistors

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ABSTRACT

In this paper we propose a new approach to operate Suppressed Sidewall Injection dual collector Magnetotransistor (SSIMT), which allows to reduce the power consumption and to implement directly switched capacitor signal-processing functions. This is obtained using charge instead of current to drive the device. Because of the clocked operation, the static power dissipation is eliminated and a sampled signal is obtained directly from the sensor. The proposed approach has been experimentally verified and the obtained results are presented.

INTRODUCTION

Dual collector bipolar magnetotransistors with suppressed sidewall injection (SSIMT) are useful sensors for medium-high magnetic field detection [1]. Since they are compatible with most IC technologies (either CMOS and bipolar), the conditioning circuitry can be easily integrated together with the sensor.

Unfortunately, the optimum operating point of this device requires a very large emitter current, in the order of some milliamperes. When it is operated in static mode, an excessive power dissipation occurs. This makes the use of SSIMT's unfeasible in many applications, such as in portable devices.

In this paper we propose a new approach to operate SSIMT's which reduces the power consumption and, in addition, allows the direct implementation of switched capacitor signal-processing functions.

SENSOR DESIGN

The basic structure of the device is shown in Fig. 2. The lateral injection of minority carriers is suppressed by a n+ guard ring all around the emitter [2].

Fig. 2- Dual collector magnetotransistor with suppressed sidewall injection structure

An important drawback of this device is the unavoidable current, $I_{SUB}$, that is collected by the substrate. This current is very strong because the corresponding vertical transistor shows a much higher current gain ($\beta_{SUB}$) than the two lateral devices ($\beta$). Typical ratios of $I_{SUB}/I_{C1,C2}$ are around 100, depending on the particular process and on the actual design of the device. Moreover, because of the n+ guard ring around the emitter which reduces the emitter efficiency [3], the lateral transistor current gain is very small and difficult to control [4].
The device was designed with an emitter collector distance of 9 µm and biased with $I_{C1} + I_{C2} = 100$ µA. The resulting parameters are summarized in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta$</td>
<td>0.05</td>
</tr>
<tr>
<td>$\beta_{SUB}$</td>
<td>1</td>
</tr>
<tr>
<td>$I_B$</td>
<td>2 mA</td>
</tr>
<tr>
<td>$I_{SUB}$</td>
<td>2 mA</td>
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</table>

**Table 1 - Electrical parameters of the SSIMT**

A measured transfer characteristic of the magnetotransistor is shown in Fig. 3. The relative sensitivity, defined as

$$ S_{r,i} = \frac{I_{C1} - I_{C2}}{(I_{C1} + I_{C2})B}. $$

is 0.45 T$^{-1}$. The offset current due to systematic mismatches is around 10 µA, which corresponds to a magnetic field of 200 mT. For our application it is interesting to express equation (1) in terms of charges. Substituting $I = Q / T$ (where $T$ is a given time interval), it results in

$$ S_r = \frac{Q_{C1} - Q_{C2}}{(Q_{C1} + Q_{C2})B}. $$

A more efficient way to control the power consumption is to use a switched capacitor circuit. In this case the magnetotransistor is charge driven and the static power consumption is eliminated. This approach is shown in Fig. 4a.

A capacitor $C_B$ is periodically charged at $(V_0 - V_{DD})$ and discharged into the base of the magnetotransistor. This produces a sharp pulse in the base current; its integral over the clock period is equal to the injected charge, $Q_B$.

$$ Q_B = \int_0^T dt = C_B(V_0 - V_{DD} + V_{BE0}), $$

where $V_{BE0}$ is the transistor base to emitter cutoff voltage, around 0.5 V.

The charge $Q_B$, is multiplied by the two lateral $\beta$ and delivered to the two collectors ($Q_{C1}$ and $Q_{C2}$) and processed. In the simple solution shown in Fig. 4b they are accumulated in two equal capacitors $C_3$ and $C_4$, until the next reset phase ($\Phi_2$). The phase $\Phi_1$ can be coincident with $\Phi_3$ (case A) or can occur with a longer period (case B).

In the former case the output voltage is given by

$$ V_{out} = \frac{1}{C_{3,4}}Q_B\beta S_B. $$

In the latter case the output charge is accumulated for $N$ clock periods, which improves the signal to noise ratio. Therefore, assuming that the magnetotransistor does not saturate, the output voltage is given by

$$ V_{out} = \frac{1}{C_{3,4}}Q_B\beta S_B N. $$

**Fig. 3-** Measured transfer characteristic of the dual collector magnetotransistor ($I_{C1} + I_{C2} = 100$ µA)

**DESCRIPTION OF THE CIRCUIT**

One possible solution to reduce the power consumption of the sensor is to use a PWM (pulse width modulation) mode of operation. However, when the device is active only for a short period of time (small duty cycle), the signal to noise ratio is degraded.
The main problem of this simple approach is that, in order to avoid the saturation of the magnetotransistor due to the big common mode charge, the integration time is limited.

\[ Q_{\text{tot},i} = Q_B B S_i + n_i, \]  

(6)

where \( n_i \) is the noise contribution and \( B \) is assumed constant. After \( N \) clock periods the output voltage can be expressed as

\[ V_{\text{out}} = \sum_{i=1}^{N} \frac{Q_{\text{tot},i}}{C_6} = \frac{1}{C_6} Q_B B S_i B N + \frac{1}{C_6} \sum_{i=1}^{N} n_i. \]  

(7)

Therefore, the noise is low pass filtered with the transfer function given by

\[ T_n = \frac{1}{C_6} \frac{\sin \left( \pi f / F_s \right)}{\sin \left( \pi f / F_s \right)}, \]  

(8)

where \( F_s \) is the clock frequency. The cut-off frequency is equal to \( F_s / N \).

The two collector charges are transferred in different clock phases. Thus, during \( \Phi_2 \) the whole common mode collector charge must be temporarily stored in the integrator. Since this charge is very large compared to the differential one, the amplifier can saturate.

**Fig. 5- Proposed solution**

Fig. 5 shows a more suitable solution. A switched capacitor integrator is used to accumulate the output charge. It is resetted during \( \Phi_2 \) every \( N \) clock periods.

The clock phases for the switches around \( C_2 \) and \( C_4 \) implement respectively an inverting and a non-inverting SC structure, allowing to integrate only the difference between the two collector charges and eliminating the undesirable common mode signal. Charges \( Q_{C2} \) and \( Q_{C4} \) are injected into the virtual ground of the integrator in phase \( \Phi_2 \) and \( \Phi_1 \) respectively. The difference is available at the end of \( \Phi_1 \).

Capacitor \( C_6 \) is resetted every \( N \) clock periods. The resulting low-pass filtering action eliminates the high frequency components of the noise, increasing the signal to noise ratio of the system. The total charge injected into \( C_6 \) for each clock cycle is given by

**Fig. 6- Experimental response of the circuit in Fig. 4b when a magnetic field is applied (\( B = 150 \text{ mT}, N = 20 \))**

To avoid this problem, we included an additional switched capacitor \( C_5 \). It does not affect the output voltage, because the average charge transfer over a clock period is zero (the capacitor is never discharged). Nevertheless it allows to compensate the large voltage swing which occurs at the output of the integrator, by properly adjusting the control voltages \( V_1 \).

For a proper operation of the circuit \( \Phi_{2n} \) must be delayed in respect to \( \Phi_2 \) and at the same time non-overlapped with \( \Phi_1 \).
The auxiliary input capacitance $C_2$ allows to compensate the offset of the magnetotransistor as well as the offset of the operational amplifier by setting a suitable control voltage ($V_d$).

**EXPERIMENTAL RESULTS**

In order to demonstrate the validity of the principle, the circuit in Fig. 4b was bread-boarded and tested. Integrated silicon sensor prototypes were used together with some discrete components. Fig. 6 shows a typical response of the circuit when a magnetic field is applied (about 150 mT). Signals 1 and 2 represent the two collector voltages, while $M1$ is their difference. It can be noticed that the common mode signal is much larger than the differential one.

Fig. 7 shows the measured transfer characteristic of the circuit. The absolute sensitivity, equal to 0.47 V/T, obtained with a common mode voltage of about 1 V and $N = 10$ is in good agreement with theoretical predictions.

![Fig. 7 - Measured transfer characteristic of the circuit in Fig. 4b ($N = 10$, $V_{C1} + V_{C2} = 2\, V$)](image)

The complete system of Fig. 5 was then integrated in a 1.2 $\mu$m single-poly, double-metal CMOS process. Fig. 8 shows a microphotograph of the chip. Two orthogonal sensors, as well as two separated interfaces, are used in order to sense also the direction of the magnetic field. The total core area is 730 $\mu$m x 690 $\mu$m. The chip is presently under testing.

**CONCLUSIONS**

In this paper we proposed a new approach to operate dual-collector magnetotransistors. We embedded the device into a switched capacitor circuit, using charge instead of current to drive it. The result is a reduction of the power consumption and the possibility to implement directly switched capacitor signal processing functions.

The principle was experimentally verified in a discrete bread-board version and a fully integrated version was designed.

The obtained experimental results demonstrated the feasibility of this approach and confirmed the theoretical predictions.

![Fig. 8 - Microphotograph of the chip](image)

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**REFERENCES**


