Design of High-Accuracy Video Comparator

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ABSTRACT
The design of high-accuracy high-frequency comparators need particular care especially with parameters such as offset and overdrive recovery. In this paper will be discussed the major design constraints and will be presented a new topology for a CMOS video comparator. The experimental results show that the proposed architecture is suitable for use in high-performance A/D converters.

I. INTRODUCTION
The interface between analog and digital domains is presently receiving ever greater attention in order to increase the resolution and operation frequency of electronic processing systems. A number of data converter architectures (such as pipeline, parallel, sub ranging, two-step flash) today allow us to improve these performances. Ultimately, however, limitations derive from the analog elementary blocks, namely the operational amplifier and the comparator.

In this paper, we focus our attention on the design of high-speed high-accuracy comparators. Until now, the requirements for CMOS comparators were limited to high resolution at a moderate speed or high speed with a medium resolution [1] - [4]. Technological advances are now pushing these limits forward and a number of processing areas are seeking speeds in the range of 50-100 MHz together with high resolution (~10 bits). When designing comparators for these applications, careful attention must be paid to speed and resolution as well as to other parameters, such as offset and overdrive recovery. This paper discusses these aspects and presents a novel architecture for CMOS comparators which meets the above requirements. Measurements on a 1.2 μm CMOS prototype show a resolution of 0.8 mV with a clock frequency of up to 80 MHz.

II. DESIGN CONSIDERATIONS
A typical comparator topology requires high-gain in an open loop configuration. To this end, either high gain amplifiers [5]-[7] or a cascade of simple inverters [8]-[10] are used.

For high-resolution, high-frequency applications we need to combine very good speed performance together with large gain. When we use a single gain stage (single pole) its output voltage \(v_{out}(t)\), in response to an applied input voltage \(v_{in}\), is given by:

\[
v_{out}(t) = g_m v_{out} v_{in} \left(1 - e^{-t/r_{out} C_L}\right)
\]

(1)

where \(g_m\), \(r_{out}\) and \(C_L\) are the input transconductance, the output resistance and the total output capacitance of the stage. For high speed operation the comparison time \(t_c\) is much smaller than the time constant \(r_{out} C_L\). Therefore, equation (1) can then be approximated by:

\[
v_{out}(t_c) = v_{in} \frac{g_m}{C_L} t_c
\]

(2)

\((g_m/C_L)t_c\) is referred to as the "dynamic gain" of the stage.
We have to note that this parameter is maximised with a large input transconductance and a minimum output capacitance.
For the cascade of \(n\) identical stages the resulting dynamic gain is equal to:

\[
\left(\frac{g_m}{C_L}\right)^n t_c^n \frac{n!}{n!}
\]

(3)

Again the optimum is achieved using a maximum possible \(g_m\) and a minimum \(C_L\) in each stage.
The required gain depends on the target accuracy that defines the minimum step at the input of the comparator. Since normally the gain stage is cascaded with a latch which requires input imbalances in the order of 20 + 100 mV, the dynamic gain needed is usually kept to below 20 + 40 dB.
An important design problem arises when large input signals are applied to the comparator. They push the amplification stage out of the normal region of operation causing a slow recovery. The time needed to recover from overdrive is unacceptable for very fast applications. This problem is normally solved by using an additional phase during which the circuit is forced to return to the normal operating point. In such a way the comparator does not keep memory of the past, and therefore the output current \((g_m v_{in})\) delivered by
the amplifying stage is entirely used to charge the load capacitance with the new data output. Another parameter to be taken carefully into account in the design of high-resolution high-speed comparators is offset voltage. Offset voltage imposes severe limits on the achievable resolution and therefore, for our applications, it must be compensated for. To this end, auto zero techniques are generally used: offset is periodically sensed, stored in a capacitor and subtracted from the processed signal. A dedicated phase is required for offset sensing and storage. A final key design problem concerns the clock feedthrough effect. The best answer for high-accuracy applications is obtained using fully differential structures. This approach minimises clock feedthrough as well as common-mode injected noise coming from coupling to power supply and uncorrelated digital signals.

III. PROPOSED ARCHITECTURE

The design issues mentioned in the previous section are solved by the architecture shown in Fig. 1. \( A_1 \) is a fully differential amplifying stage, which drives an output differential latch. \( A_2 \) is an auxiliary amplifier for the offset cancellation loop.

Three non-overlapping phases control the comparator. Phase \( \Phi_1 \) is used for the comparison. The signal is applied at the input of the gain stage during \( \Phi_1 \). At the end of the phase, the output voltage is stored in the input capacitance of the latch (\( C_5 \) and \( C_6 \) reset during \( \Phi_1 \) and strobed by phase \( \Phi_2 \). Phase \( \Phi_2 \) is the reset phase (overdrive recovery of the gain stage). To this end, both the input and the output terminals of the amplifier are short circuit; this ensures a fast discharge of the output nodes, regardless of previous conditions.

Fig. 1. Proposed comparator architecture; \( \Phi_1, \Phi_2 \) and \( \Phi_3 \) are non-overlapping phases.

Phase \( \Phi_3 \) is used for offset compensation. The input terminals of the gain stage remain short circuited while the outputs are left free. The input offset is amplified and, after sampling and low-pass filtering by means of a switched-capacitor section (SC Filter) it is further amplified by \( A_2 \). The output of \( A_2 \) modifies an auxiliary input of \( A_1 \) which controls the offset.

For high speed high accuracy operation we have simply to design a gain stage \( A_1 \) with the required dynamic gain. Overdrive recovery is ensured by the switches at the input and output of \( A_1 \), the offset is cancelled with the feedback loop including \( A_2 \) and the clock feedthrough is compensated by a fully differential architecture.

IV. CIRCUIT IMPLEMENTATION

Fig. 2 shows the circuit schematic of the amplifier and the offset compensation loop, together with the biasing circuit. \( A_1 \) is a differential stage with fully differential output. Its common-mode feedback (CMFB) is realised with a continuous-time loop. The output common-mode voltage is detected by the pair \( M_6-M_7 \) (node 3), and adjusts the current flowing through MCM. The use of the two transistors \( M_5 \) and \( M_7 \) allows better CMFB control even with a high bias current in the differential stage. The poor linearity of the CMFB used has no relevant effect in our application in that it privileges speed.

The auxiliary input is achieved by adding to the active loads \( M_3 \) and \( M_4 \) the transistors \( M_{11} \) and \( M_{12} \) kept in the triode region.

Two n-channel transistors (\( M_{D1}, M_{D2} \)) are the switches for the overdrive recovery. They also perform an additional function: to avoid large swings at the output of the amplification stage, they become two parallel back-to-back diodes during \( \Phi_1 \). \( M_{D1} \) and \( M_{D2} \) are made into switches or diodes by the action of transistors \( M_{C1} \) to \( M_{C4} \). The overall diode switch (D/S) structure is enclosed within a dashed box in Fig. 2.

The outputs of \( A_1 \) are sampled during the offset cancellation phase by a switched capacitor low pass filter before entering the offset compensation amplifier \( A_2 \).

To relax the capacitor ratio the SC sampling and filtering section is driven by phases \( \Phi_3 \) and \( \Phi_1 \), which are synchronous with the main phases \( \Phi_2 \) and \( \Phi_1 \), but whose rate is lower by a factor of 16. Finally, stage \( A_2 \) completing the offset compensation loop is a simple differential stage (transistors \( M_{13} \) to \( M_{17} \)). The design conditions mandate high transconductances \( g_{m1} \) and \( g_{m2} \) and low capacitances at nodes (1) and (2). The first condition leads to relatively wide input transistors (\( W/L = 180/1.2 \)) while the second justifies the use of source followers (\( M_{9-10} \) (\( M_{11-12} \)). The capacitance affecting node (1) and (2) is equal to

\[
Cp1 = C_{dgm1} + C_{dgm1v} + C_{dmb1} + C_{dgm3} + C_{dgm3v} + C_{dmb3} + C_{gsMD1} + C_{gsMD1v} + C_{gbsMD1} + C_{dgmMD2} + C_{dgmMD2} + C_{gsMC3} + C_{gsMC3v} + C_{gbsMC3}
\]
For the designed circuit $C_p1 = 0.38 \, \text{pF}$ and $g_m = 2 \, \text{mA/V}$ and therefore, the dynamic gain ($t_c = 4 \, \text{ns}$) is approximately 26 dB. This number is sufficient to drive the latch. Fig. 3 shows the circuit diagram of the latch. It is made up of an n-channel flip-flop, a p-channel flip-flop, two transfer gates for strobing, and two output inverters. Compared with previous realisations [12] both the n-channel and the p-channel regenerative stages each contain a couple of reset transistors. This solution increases the speed of operation and avoids hysteresis. In addition the capacitive load of nodes (31) and (32) are reduced by the use of two output inverters (transistors M30 to M33).

V. EXPERIMENTAL RESULTS

The circuit was fabricated using a 1.2 $\mu$m CMOS process. Its microphotograph is shown in Fig. 4. The layout has the shape shown to favour its use in an array as is required for flash and two-step flash converters. The active area is 130 mils$^2$.

Experimental results refer to a power supply $V_{DD} = 5 \, \text{V}$ and an output capacitive load of 0.3 pF; this value corresponds to a logic section of medium complexity. The speed achieved is 80 MHz (3 phases of 4 ns each) with a sensitivity, measured with a common mode input ranging from 1.5 V to 3.5 V, which is always below 0.8 mV. Table I shows the performance of the circuit.

We note that the simple scheme of $A_1$ and the relatively high bias current (300 $\mu$A) allows a very high bandwidth. With 0.8 mV at the input, we can obtain an imbalance at the input of the latch equal to 16 mV in only 4 ns. This is enough to produce full switching in a further 4 ns. Fig. 5 shows the delay between the strobe signal ($\Phi_2$, smoothed by the capacitive load of the probe) and the output of the latch in the operating conditions described above.
specially designed offset cancellation loop. The characteristics obtained make the proposed comparator suitable for use in high-performance mixed circuits such as high-frequency A/D converters.

ACKNOWLEDGMENT

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REFERENCES


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<td><strong>FIRST STAGE DC GAIN</strong></td>
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<td><strong>FIRST STAGE GAIN BANDWIDTH</strong></td>
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<tr>
<td><strong>RESOLUTION</strong></td>
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<td><strong>OFFSET REDUCTION FACTOR</strong></td>
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<tr>
<td><strong>POWER DISSIPATION (VDD = 5 V)</strong></td>
<td>6.5 MW</td>
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Table 1 - Typical performance of the proposed comparator.