TEACHING FULL-CUSTOM DESIGN OF ANALOG BUILDING BLOCKS WITH EUROCHIP FACILITIES

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ABSTRACT

This paper presents an experience in teaching analog microelectronics at the University of Pavia. Facilities provided by EUROCHIP were exploited in the Microelectronics course, to train undergraduate students in the field of full-custom analog circuit design. Laboratory exercises consist of the design of CMOS operational amplifiers, including simulation with SPICE and layout with Cadence Edge. The circuits designed were integrated in the MITEC 2.4 μm technology.

I – INTRODUCTION

The Faculty of Engineering at the University of Pavia offers courses leading to a first-level degree (Diploma) in electronic engineering, in computer engineering, in biomedical engineering, in infrastructure engineering and in environmental engineering. It also offers courses leading to a second-level degree (Laurea) in electronic engineering, in electrical engineering, in computer engineering, in civil engineering, in environmental engineering and in construction engineering.

The second-level degree in engineering is spread over five years. During the first two years, lectures provide a common background and most of the teaching resources are shared between all courses of the faculty. The last three years are devoted to curriculum specialisation. Regarding the degree in electronic engineering, they include basic electronics courses, which are mandatory, together with more specialised courses which can be chosen by students according to their choice of curriculum. The branches of specialisation in electronic engineering are: Telecommunications, Instrumentation, Optoelectronics and Microelectronics.

II – THE MICROELECTRONICS CURRICULUM

The curriculum in Microelectronics at the University of Pavia is characterised by a specialisation in the design of analog integrated circuits. This is not common for Italian
universities, which usually provide only fundamentals of analog design and instead concentrate more on teaching digital design.

The fundamental courses in the Microelectronics curriculum are:

- ‘Electronics I’,
- ‘Electronics II’,
- ‘Electronics III’,
- ‘Technology and Materials for Electronics’,
- ‘Electronic Devices’, and
- ‘Microelectronics’.

In the academic year 1994/95, the course of ‘Design of Digital Integrated Circuits’ will be activated.

At completion of the principal courses the student is involved in researching a thesis, which usually lies within the frame of a research project.

The basic idea behind the Microelectronics curriculum is to provide students with a solid background in silicon technology and circuit design. This is achieved by courses on ‘Electronics II’, ‘Electronic Devices’ and ‘Technology and Materials for Electronics’. The last course links basic background to more practical issues that are also partially dealt with in the ‘Microelectronics’ course (described in details below) and in a future course on ‘Design of Digital Integrated Circuits’. With the practical courses we seek to provide on-the-job knowledge. For this reason, the courses are heavily focused on exercises, use of CAD tools and practical sessions.

The response of the industrial environment is quite positive: most of our students quickly find a job as circuit designer for the major silicon producers and users located in the area. Despite its relatively small size, our school in analog electronics is well known throughout Italy and abroad, and has an excellent reputation.

III - THE MICROELECTRONICS COURSE

The ‘Microelectronics’ course is devoted to students in Electronic Engineering in the last year of their curriculum. Being placed in the first semester of the fifth year, after the basic electronic courses, the ‘Microelectronics’ lectures provide a review of MOS transistor operation and introduce students to the design of analog blocks and subsystems. The course has a duration of 80 hours and covers the following topics:

- behaviour and modelling of the MOS transistor (also considering the weak inversion region);
- passive components and switches in CMOS technology;
- design of CMOS analog building blocks: inverter, cascode, differential stage, source follower, output stages, level shift, current mirrors, current and voltage references;
- design of CMOS operational amplifiers and comparators;
- continuous-time and switched-capacitor filters;
- A/D and D/A converters.

Laboratory activities integrate the lectures with practical exercises on analog design. To introduce undergraduate students to full-custom analog design, exercises must deal with simple and small building blocks. For this purpose, some operational amplifier architectures have been chosen.

About 25 students were involved in the laboratory activities. They were divided into working groups, each of which was composed of more or less 4 people. Each group had to study an op-amp architecture. The tasks were:

- calculation of first component sizing from theoretical relationships;
- verification of circuit performance with a circuit simulator, and tuning of
geometrical parameters;

* design of the layout of the op-amp.

The lecture notes [1] and the textbook [2] were used for first order component sizing. Circuit simulations were performed using SPICE 2.G or PSpICE*. During this phase, students had the opportunity to evaluate the effects of design parameter variations, such as dc gain and output resistance dependence on the bias current in transconductance amplifiers. Following this they could compare the simulated results with the theory, also evaluating higher order effects. After verifying op-amp performance (operating point, power dissipation, dc gain, unity gain frequency, phase margin and output dynamic range), the layout of the circuits was realised using the layout editor of the Cadence Edge 2.1f. package. Six op-amps were designed and four of them were integrated using MITEC 2.4 μm technology which is suitable for full-custom designs. Two circuits contained layout errors and the semester ended before we could submit the correct designs on time.

IV – THE ROLE OF EUROCHIP IN MICROELECTRONICS TRAINING

Facilities provided by EUROCHIP play an important role in microelectronics student training. The availability of modern CAD tools allows us to better qualify graduate students for a job as circuit or system designers. Silicon prototype fabrication is also an important aspect of the training, since it requires students to deal with practical design aspects (such as component matching and symmetry, crosstalk, power supply lines, substrate bias, pad protection and pin configuration) which are usually neglected in theoretical circuit analysis.

The major problems encountered during this teaching experience are due to the very strict time limit imposed by the semester. Since the laboratory exercises must take place after the lectures on op-amp design, the layout is done in the very last part of the course and there is no time for layout modification in case of error or design rule violations. Moreover, silicon prototypes are delivered after the end of the course, when students are heavily involved in the last semester courses. This prevents us from testing the silicon prototypes during laboratory sessions, which would be a very rewarding experience for students.

Despite these drawbacks, the global evaluation of this training is very positive. Although the time required for the course was slightly increased by practical exercises, students were very much in favour of this initiative. Many of them decided to choose a microelectronics design activity for their degree thesis. The practical work during the 'Microelectronics' course reduced the need for additional training in VLSI design during the thesis, increasing the time available for research.

V – DESIGN EXAMPLES

A brief summary of the operational amplifiers selected for student designs is shown in Table I.

Specifications were intentionally left incomplete, so that only a few requirement needed to be satisfied by students. Besides dc gain and bandwidth or load capacity requirements, the only limits were a single 5 V power supply and a suggested power dissipation not exceeding 1 mW. Loose specifications gives more time to explore the

* We observed that the work done by students having a PC equipped with PSpICE at home was much more exhaustive in simulations.
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<th>Name</th>
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| OP1    | Folded-cascode OTA                              | DC gain: $A_0 > 90$ dB  
GBW: $f_T = 30$ MHz                            |
| OP3    | Single-stage telescopic OTA                     | DC gain: $A_0 > 90$ dB  
GBW: $f_T = 100$ MHz                            |
| OP5    | Two-stage op amp with MOSFET-C compensation     | DC gain: $A_0 > 80$ dB  
Max capacitive load: $C_L = 10$ pF            |
| OP6    | Two-stage class AB op amp                       | DC gain: $A_0 = 90$ dB                              |

potentialsities of the simulation tool in different types of analysis.

The op-amp layout can be designed using the full-stacked approach, which lead to compact and symmetrical layouts with reduced parasitics [3].

Schematic diagrams of the four op-amps are drawn in Fig. 1. Fig. 2 summarises the simulation results obtained by the student group working on OP5. Finally, Fig. 3 shows the op-amp core layouts designed by students with the full-stacked approach.

![Schematic diagrams of the op-amps](image_url)

Fig. 1 - Schematic diagrams of the op-amps
Fig. 3 - Full-stacked layout of the op-amps

REFERENCES


VI - CONCLUSION

We experienced that EUROCHIP facilities can help improving undergraduate student training in the design of analog blocks. Although analog design is more time-consuming than digital design, small analog building blocks such as op-amps can be designed by students in a class semester, from simulation to full-custom layout.

This kind of exercises has been greatly appreciated by students involved in this activity, and allowed us to increase the training quality. The satisfactory results obtained with this experience confirm that the teaching approach was correct.