A Hall Sensor with Current-Controlled and Improved Sensitivity

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ABSTRACT

In this paper we present a novel split-current magnetic sensor (bulk Hall plate operated in the current mode) with on-chip circuitry, fabricated in an industrial 2 μm CMOS process. The sensor consists of a low-doped resistive path with one input and three output terminals. The on-chip circuit controls the biasing of the sensor, performs the difference between the currents flowing through the outer output terminals and provides an output voltage proportional to the applied magnetic field. We demonstrate that the sensitivity and the noise performances of the proposed device can be tuned by changing the ratio between the bias currents applied to the input and to central output terminal, while keeping constant the power consumption. Numerical simulations based on a finite element method and experimental results on an integrated prototype are reported.
I. INTRODUCTION

Magnetic sensors are used in many industrial and domestic applications. Most of them are based on the Hall effect, which exploits the deflection of moving electrical charge carriers due to the Lorentz force in the presence of a magnetic field. Different kinds of devices have been proposed, operating either in voltage or current mode. Current mode magnetic sensors are for example dual collector magnetotransistors [1], double or triple drain MAGFETs [2] and split-current Hall plates. They are usually compatible with standard IC technologies (CMOS or bipolar) [3] and therefore they are very promising in view of batch-fabrication and co-integration with interface circuitry.

All these devices share the same operating principle: without magnetic field the current applied at the input terminal \( (I) \) is symmetrically divided between the output terminals. However, in the presence of a magnetic field the Lorentz force introduces an asymmetry and causes a current imbalance \( (\Delta I) \) which is proportional to the magnetic induction \( (B) \).

Therefore, for current mode magnetic sensors the absolute sensitivity is always defined as

\[
S_a = \frac{\Delta I}{B}.
\]

However, a more significant figure of merit is the relative sensitivity,

\[
S_r = \frac{S_a}{I_{I_B=0}} = \frac{\Delta I}{B I_{I_B=0}},
\]

which represents the relative current difference with respect to the common mode current. This information is very important when a read-out circuit is associated with the sensor because it determines the required dynamic range.

In this paper we propose a novel split-current magnetic sensor with on-chip biasing and read-out circuit, fabricated in an industrial CMOS technology. The sensitivity and the signal-to-noise ratio of the proposed sensor can be controlled by changing the bias currents, while keeping constant the total current (and therefore the power consumption). This allows us to cover a wide range of magnetic fields using the same device and the same interface circuit.
II. DEVICE DESCRIPTION AND THEORY OF OPERATION

The proposed device belongs to the category of split-current Hall magnetic sensors. The structure consists of a low-doped resistive path formed by an n-well with one input and three output terminals. The size of the n-well is 40x40 μm and the spacing between the output terminals is 15 μm. Layout and cross-section of the device are shown in Fig. 1. A shallow p+ diffusion on top of the n-well and contacted to the substrate (V_{SUB}) increases the resistivity of the conductive layer. Moreover, it prevents current conduction along the Si/SiO₂ interface, reducing the low-frequency flicker noise due to surface traps.

In order to operate the device, a fixed current, I_{TOT}, is applied to the input terminal (S_{in}). With a second current source we control the current I_j < I_{TOT} extracted from the central output terminal (S_j). Without an external magnetic field the residual current I_2 = I_{TOT} - I_j is equally divided between the two outer output terminals (S_f and S_2). In the presence of a magnetic field perpendicular to the chip plane (B_z), the current in the n-well is deflected due to the Lorentz force acting on the electrons. This leads to a current difference ΔI between S_f and S_2, which is given by [4]

$$\Delta I = G \mu_H \frac{L}{W} I B_z,$$

where $\mu_H$ is the Hall mobility, $G$ is a correction factor which takes into account geometrical non-idealities, while $L$ and $W$ are respectively the length and the width of the conductive layer.

If we look carefully to eqn. (3), we see that the current difference, and therefore the sensitivity of the device, can be expressed as a function of the current density in the n-well ($J_x$). In fact, $\Delta I$ can be written as

$$\Delta I = G \mu_H J_x L t B_z,$$

where $t$ is the thickness of the conductive path.

Usually in a Hall device operated in the current mode $J_x$ depends only on the total current flowing into the sensor (I_{TOT}) and on its geometry (W). However, in this particular structure, if we increase $I_j$, keeping $I_{TOT}$ constant, the current is confined in the central area of the device and therefore $J_x$ is increased. On the other hand, if we reduce $I_j$, the current spreads across the
whole sensor width, thereby reducing $J_x$. It is therefore possible to control the current density and tune the sensitivity of the device simply by changing current $I_j$, while maintaining constant the power consumption.

We verified this effect by simulating the proposed sensor with a two dimensional finite element program (SESES [5] [6]). Fig. 2 shows the current density in the device for $I_j = 50 \mu A$ (a) and $I_j = 90 \mu A$ (b). In both cases $I_{TOT} = 100 \mu A$. It can be observed that with $I_j = 90 \mu A$ the current is concentrated in the center of the device, as expected.

A further consequence of this effect is that the actual resistance of the lateral paths, defined as

$$R = \frac{V_{S_{u}} - V_{S_{l,2}}}{I_2},$$

increases with $I_j$, as demonstrated by the measurement shown in Fig. 3.

III. SENSITIVITY AND NOISE ANALYSIS

Taking into account the current density modulation mentioned in the previous section, we can approximate the sensitivity of the device with a linear expression given by

$$S_a = \frac{\alpha_1 \cdot I_1 + \alpha_2 \cdot I_{TOT}}{B} ; \quad I_1 < I_{TOT},$$

where $\alpha_2$ accounts for the increasing applied current, while $\alpha_1$ represents an additional term due to the concentration of the current in the center of the device (i.e. the reduction of the effective $W$). We verified these assumptions with numerical simulations (SESES), obtaining a perfectly linear behavior with coefficients $\alpha_1$ and $\alpha_2$ equal to 0.024 and 0.0246 respectively.

Eqn. (6) shows that $S_a$ is minimal for a given $I_{TOT}$ when $I_j = 0$ and it increases when we increase $I_j$. The case $I_j = 0$ corresponds to a conventional structure with two output terminals. The relative sensitivity for this particular device is given by

$$S_r = \frac{\alpha_1}{B} \frac{I_1}{I_{TOT} - I_1} + \frac{\alpha_2}{B} \frac{I_{TOT}}{I_{TOT} - I_1} ; \quad I_1 < I_{TOT}.$$  

When $I_j = 0$, $S_r$ is minimal, constant and independent of $I_{TOT}$. By increasing $I_j$, while
maintaining $I_{TOT}$ (and thus the power consumption) constant, we can increase the relative sensitivity as much as we need to fit the requirements of the following read-out circuit.

However, the relative sensitivity is not the ultimate figure of merit for the resolution of the sensor. In fact, in order to determine the minimum detectable magnetic field ($B_{min}$) we have to consider the signal-to-noise ratio (SNR), defined as

$$SNR = \frac{(\Delta I)^2}{N} = \frac{(S_a B)^2}{N},$$

where $N$ represents the noise power in the band of interest. By definition $B_{min}$ is the value of $B$ which satisfies the condition $SNR = 1$. It is given by

$$B_{min} = \frac{\sqrt{N}}{S_a}.$$  \hspace{1cm} (9)

We can analyze the noise performances of the proposed device using the simple equivalent circuit shown in Fig. 4. The sensor is modelled with three noisy resistors representing the conductive paths, while current sources are replaced by their noisy output resistances. Moreover, $V^2_{n,ref}$ summarizes the noise contributions from the biasing and read-out circuit.

Looking at this circuit we see that noise sources $V^2_{n,I}$, $V^2_{n,lI}$ and $V^2_{n,ref}$ give rise to fully correlated contributions in the two output currents ($I^2_{n,1}$ and $I^2_{n,2}$). Therefore, since we are interested only in the differential signal they can be neglected. Assuming that $R_{IT}$ and $R_{II}$ are much larger than $R$ the output noise due to $V^2_{n,1}$ and $V^2_{n,2}$ is given by

$$I^2_{n,out} = \frac{V^2_{n,1} + V^2_{n,2}}{4R^2}.$$  \hspace{1cm} (10)

Since $V^2_{n,1}$ and $V^2_{n,2}$ are thermal noise contributions ($V^2_{n,1} = V^2_{n,2} = 4kTR\Delta f$), $I^2_{n,out}$ can be written as

$$I^2_{n,out} = \frac{2kT\Delta f}{R}.$$  \hspace{1cm} (11)

Eqn. (11) shows that the output noise is inversely proportional to the lateral resistances ($R$). Therefore, the SNR increases as we increase $I_I$, not only because we improve the sensitivity of the device, but also because we reduce the noise ($R$ increases with $I_I$).

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IV. CIRCUIT DESCRIPTION AND EXPERIMENTAL RESULTS

The block diagram of the biasing and read-out circuit integrated together with the sensor is shown in Fig. 5. It consists of two current sources ($I_{TOT}$ and $I_f$) which provide the bias current, a feedback loop ($A$, $M_4$ and $M_f$) which controls the voltage at terminals $S_1$ and $S_2$ and a degenerated current mirror ($M_2$, $M_3$, $M_5$ and $M_6$) which performs the difference between the output currents.

By changing $V_{ref}$ we can set the correct voltage at the output terminals, while maintaining transistors $M_f$ and $M_4$ properly biased. The currents flowing out from terminals $S_1$ and $S_2$ are collected by the sources of $M_f$ and $M_4$ and provided to the current mirror. $V_R$ allows us to set the quiescent value of the output voltage.

We integrated the proposed sensor as well as the biasing and read-out circuit in a standard 2 µm CMOS process. A microphotograph of the chip is shown in Fig. 6.

Fig. 7 shows the measured transfer characteristic of the sensor biased with $I_{tot} = I_f = 50$ µA. It can be observed that the curve is very linear, as expected. The absolute and the relative sensitivity of the device as a function of $I_f$ are reported in Fig. 8. The measured curves are in good agreement with eqns. (6) and (7) and with numerical simulations. The obtained values for coefficients $\alpha_1$ and $\alpha_2$ are 0.027 and 0.052, respectively.

Finally Fig. 9 shows the output voltage of the read-out circuit as a function of the applied magnetic field. The sensor was biased with $I_{tot} = I_f = 50$ µA. Also in this case the curve is very linear.

V. CONCLUSIONS

In this paper we presented a novel split-current magnetic sensor with on-chip biasing and read-out circuit. Since the sensitivity and the noise performances of the sensor are electrically tunable, this device is suitable for wide dynamic range magnetic field measurements. For example we foresee possible applications in contactless line current measurements. The sensor and the circuit were integrated in a standard 2 µm CMOS technology. The obtained experimental results are in very good agreement with theoretical predictions and with...
numerical simulations.

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REFERENCES


FIGURE CAPTIONS

Fig. 1 - Layout (a) and cross-section (b) of the proposed sensor

Fig. 2 - Simulated current densities in the proposed device with $I_{TOT} = 100 \, \mu A$ and
(a): $I_I = 50 \, \mu A$, (b): $I_I = 90 \, \mu A$

Fig. 3 - Measured resistance of the lateral conductive paths in the proposed sensor as a
function of current $I_I$ with $I_{TOT} = 100 \, \mu A$

Fig. 4 - Noise equivalent circuit of the proposed sensor

Fig. 5 - Biasing and read-out circuit

Fig. 6 - Microphotograph of the chip

Fig. 7 - Measured transfer characteristic of the proposed sensor

Fig. 8 - Measured absolute and relative sensitivity as a function of $I_I$ with $I_{TOT} = 100 \, \mu A$

Fig. 9 - Measured transfer function of the proposed sensor with the biasing and read-out circuit
Fig. 1

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Fig. 2

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$I_{tot} = 100 \mu A$

Fig. 3

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Fig. 4

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Fig. 5

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Fig. 7

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$I_{\text{tot}} = 100 \, \mu\text{A}$
Slope $= 2.7 \times 10^{-5} \, \text{mT}^{-1}$

$S_a [\mu\text{A/mT}]$

$S_r [\mu\text{A/mT}]$

$I_1 [\mu\text{A}]$

Fig. 8

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Fig. 9

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