Motion detection with an intelligent optical sensor with on-chip analogue memory

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Abstract

A 64 x 64-pixel image sensor with full-frame analogue memory and on-chip motion processor is presented. The processor, consisting of a charge amplifier and an analogue subtractor realised with a switched capacitor technique, calculates the difference between the values of the signal on each pixel in successive frames at a rate of up to 60 frames/s with limited area and power overhead. Fabricated in a 1.2 μm standard CMOS process with an added metal 3 light-shielding layer, the circuit is fully functional and requires a total core area of 13 mm².

1. Introduction

Optical sensor systems including intelligent processing of signals for specialised applications are emerging. In a number of systems we have the requirement of motion detection [1] for activating successive functions. A typical example is in the surveillance area, where the intrusion of an object in an otherwise stationary scene should activate a closer examination of the alerted area. Motion detection can be achieved by digital processing of the signal at the output of a conventional camera; however, the complexity and speed of the computational circuitry required make the cost of the system unacceptable. For this reason, a dedicated optical sensor system is a suitable solution for specialised applications.

This paper describes an integrated circuit that performs the functions required for motion detection using an analogue motion processor and an on-chip analogue memory to store the information of the previous frame. A limited spatial resolution is sufficient in the machine vision tasks at hand as only general information on the motion contents of the scene is required, as opposed to a high-resolution image.

2. Circuit description

The architecture of the sensor comprises a square array of 64 x 64 photosensors and analogue memory cells. Cell selection is achieved by two decoders [2] which select one cell at a time and connect it to the motion processor as depicted in the block diagram, Figure 1. The motion processor, which includes an offset-insensitive amplifier and an analogue subtractor to provide directly the difference between one frame and the previous one, is described in more detail below. An output buffer at the output of the processor drives the capacitance of the I/O pad.

Photosensor/memory cell. The layout of the basic sensing cell is shown in Figure 4. We can identify the photodiode realised with an n+/p junction [2] and the storage capacitor consisting of poly over an implanted active area. The size of the photodiode is 40 μm x 25 μm, and the size of the capacitor is 35 μm x 15 μm. The cell also includes selection switches implemented with n-channel transistors with a size close to the minimum,
w = 2 μm, l = 1.5 μm, to minimise the leakage current. The size of the basic sensing cell is 48 μm x 48 μm, which leads to a 64 x 64-cell array size of 3.2 x 3.3 mm² including the two selection decoders and column switches. The memory cell is contiguos to the photodiode for reasons of equalisation of the stray capacitance on the long lines connecting the charge amplifier to the photodiode/storage capacitors within the array. This topology also saves a space-consuming extra decoder for the capacitor array, although the memory bank could be placed outside the light-sensitive area, with the advantages of a reduced sensitivity and smaller charge leakage in the presence of strong illumination conditions.

**Motion processor.** The subtraction of the signal from two successive frames is carried out by the switched-coupling motion processor (Figure 2). This consists of two stages: a charge amplifier (op-amp A1) which converts to voltage the charge stored in the photosensor in the memory cell and pushes the pixel charge back into the corresponding memory capacitor. The second stage is a subtractor (op-amp A2) which computes the difference between the signal stored in the memory capacitor during the previous scanning period (i-1) and the signal produced by the photodiode in the present one (i). The charge amplifier and the subtractor operate in four basic cycles. During the first cycle (φ1), the charge stored in the analogue memory, CM, is integrated by the charge amplifier, that produces an output voltage

\[
V_{X1}(i, φ1) = V_{REF1} + \frac{CD}{Cl}(V_{REF3} - V_{CD}(i-1))
\]

that is loaded on the capacitor C2. The second cycle (φ2) is used to pre-charge the capacitor C1 to the voltage VREF3 + VREF1 (neglecting offset). During the third cycle (φ3) the charge amplifier integrates the charge stored in the selected photodiode and produces an output voltage

\[
V_{X1}(i, φ3) = V_{REF1} + \frac{CD}{Cl}(V_{REF3} - V_{CD}(i))
\]

that produces a voltage variation \(V_{X1}(i, φ1) - V_{X1}(i, φ3)\) on the inverting-input of the second stage. In this way the output of the second stage takes the difference between the value read during φ1, (previous frame) and the value read during φ3 (present frame):

\[
V_{out}(i, φ3) = V_{REF2} + \frac{CD}{Cl} \frac{C2}{C3} (V_{CD}(i) - V_{CD}(i-1))
\]

The photodiode is automatically reset to VREF3 as required for the next charge integration period. The fourth cycle is used to push the charge from the amplifier back into the memory capacitor. In this way the memory capacitor of the cell stores the value of the previous frame while C1 is precharged to (VREF3 - VREF1). Reset of the feedback capacitor C3 is performed during φ1 and φ4. The operation of the charge amplifier and of the subtractor stage is offset-insensitive [3]. A folded-cascade topology has been adopted for A1 and A2 (gain = 80 dB; GBW = 19 MHz, slew rate = ±10 V/µs with CL = 6 pF; power consumption = 1.7 mW). VREF1, VREF2 and VREF3 were set equal to 1.5 V, 2.5 V and 3 V respectively. The nominal voltage gain of the charge amplifier and of the subtractor were set equal to unity (C0 = C1 = 0.2 pF) and to 0.5 (C2 = 0.5 pF, C3 = 1 pF) respectively. The approach used allows the calculation of the signal of the present frame, the previous frame and their difference. Therefore, we can achieve an excellent flexibility for fulfilling different functional requirements.

**3. Results**

The circuit was fabricated in a 1.2 μm, n-well, single-poly silicon, implanted-capacitor double-metal CMOS technology by MITEC with the addition of a special metal 3 layer over the passivation acting as a light shield to reduce the effect of carrier generation in the analogue circuits outside the photosensor array in the prevailing condition of non-uniform illumination. Chip area is 6.8 x 6.8 mm² (Figure 3). Experimental tests show
that the circuit is fully functional. Total current consumption is 2.4 mA at 5 V, with about 900 μA supplied to the analogue circuits and about 1.5 mA for the digital section. The readout section of the array and motion processor were tested separately from the array in a specially-designed test chip which enabled an electrical signal to be injected into the input of the motion processor. The input and output waveforms resulting from one of the tests are depicted in Figure 5, where the peaks in the output signal (top) represent the first time derivative of the excitation signal (bottom). The difference is taken between the signal at sampling time \( t_n \) and the previous signal at sampling time \( t_{n-1} \). A preliminary test on the complete array is in good qualitative agreement with the theoretical behaviour at a frame rate of up to 60 frames/s. Typical applications are in the triggering of alarm signals in the presence of intruders in an otherwise stationary scene and direction control of moving vehicles by non-contact optical sensors.

4. Conclusion
The feasibility of simple motion detection obtained with inexpensive analogue processing was demonstrated by an experimental chip. Operation was tested at up to 60 frames/s. This performance was achieved with limited circuitry having a small area and power overhead as compared to the photosensor array. The analogue memory increases the area of a pixel site by about 40% only. Similar performance in a digital solution would require a processing power of hundreds of thousands of operations per second, a larger silicon area for the processor and the digital memory and considerably higher power.

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References

Figure 1. Simplified block diagram of chip
Figure 2. Schematic of one photodiode/memory cell with motion processor

Figure 3. Microphotograph of the chip

Figure 4. Layout of the photodiode/memory cell

Figure 5. Operation of the motion processor in the time domain with an electrical excitation on the amplifier. The peaks in the output signal (top) are proportional to the first time derivative of the input (bottom).