High Dynamic Range Interface System for a Micromachined Integrated AC-Power Sensor

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ABSTRACT
This paper describes a read-out system for a CMOS compatible integrated AC-power sensor. The system consists of two equal micromachined devices operated at the same power level in a closed loop configuration. The large dynamic range requirements are met by a novel oversampled A/D converter embedded in the feedback loop. The system uses a variable reference voltage, which is controlled and measured on chip. The large thermal time constant of the sensor introduces additional stability problems in the non-linear system. Therefore, we optimized the proposed architecture by non-linear analysis and numerical simulations. The complete system including the sensor was implemented in a 2 μm CMOS process on a single chip.

INTRODUCTION
Thermocouplers are used for AC-power measurements in microwave instrumentation and true mean square voltage evaluation. Recently, micromachined integrated thermocouplers have been proposed [1] [2], allowing the advantages of batch fabrication and on chip electronics to be combined in a cost-effective micro-module.

The schematic of a CMOS compatible micromachined AC-power sensor is shown in Fig. 1. When an AC signal is connected to the heating resistor, the dissipated power produces a temperature gradient. A thermopile consisting of p- and n-doped polysilicon lines detects the temperature difference and through the Seebeck effect provides an output voltage proportional to the mean square value of the input signal. To increase the sensitivity of the device, the bulk silicon is etched under the sensor structure creating an oxide membrane, which ensures low thermal conductivity between the heating resistor and the cold junctions of the thermopile.

The electrical parameters and the performance of the sensor are summarized in Table 1. It can be observed that the dynamic range of the device covers four orders of magnitude, from 1 μW to 10 mW. Therefore, to preserve the overall performance of the system, this wide dynamic range is also required for the interface circuitry, making its design in CMOS technology very challenging. Oversampling and noise shaping techniques are very suitable for this application, since they allow to achieve high performance in terms of signal-to-noise ratio, resolution and linearity, without needing accurate analog component matching [1].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Membrane size</td>
<td>500 μm x 1000 μm</td>
</tr>
<tr>
<td>Heating resistor</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>Thermopile resistance</td>
<td>750 kΩ</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>113 V/W</td>
</tr>
<tr>
<td>Time Constant</td>
<td>10 ms</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>1 μW + 10 mW</td>
</tr>
</tbody>
</table>

Table 1 - Electrical parameters and performance of the integrated CMOS power sensor
SYSTEM ARCHITECTURE

The block diagram of the proposed system is shown in Fig. 2. It consists of two thermoconverters operated in a closed loop configuration. The input signal \( v \) is connected to one sensor, while the feedback signal \( f \) is connected to the other. The difference between the two output voltages \( e \) is delivered to the interface circuit, processed and fed back. Since the loop gain is large, system operation forces both devices to the same input power level. Therefore, any deviations in the transfer characteristic of the sensors are mutually canceled. In particular, the non-linearity appearing at high power levels due to the thermal coefficient of the heating resistor, is compensated.

The interface circuit consists of a sampled-data controller, \( G_2(z) \), and a latched comparator, operated at high clock frequency (oversampled). The bitstream provided at the output \( s \) is multiplied by the reference voltage \( t \) and fed back to the reference sensor. Because of the large gain of the loop and the low-pass transfer function of the sensor, the mean value of the bitstream is proportional to the power of the input signal. Moreover, for a given input signal, the average frequency of the bitstream \( f_{bh} \) is proportional to the reference voltage \( t \).

Unfortunately, when the level of the input signal is low and \( f_{bh} \) becomes smaller than the cut-off frequency of the sensor \( f_{sens} \), the behavior of the system changes and an error occurs. In order to overcome this problem, we introduced an additional signal path which adjusts the reference voltage \( t \) according to the input signal, thus keeping \( f_{bh} \) larger than \( f_{sens} \) under any operating conditions. To this end, the true mean square value of the input signal is roughly measured using the sensor in open loop configuration. The resulting voltage \( q \) is used to generate the reference voltage while, at the same time, it is converted into the digital domain by an incremental A/D converter [3][4]. The digital word obtained \( N_{ad} \) is modulated with the bitstream \( s \) and then decimated and filtered. As a result, the digital representation of the input signal power becomes independent of the actual value of \( t \).

The noise shaping function and the stability of the system are determined by the transfer functions of the controller, \( G_2(z) \), and the sensor, \( G_1(s') \). In order to obtain the required signal-to-noise ratio and ensure the stability of the system under any operating conditions, \( G_2(z) \) has to be carefully designed.

SYSTEM ANALYSIS

The sensor can be modelled by a squarer followed by a linear first order transfer function

\[
G_1(s') = \frac{\beta}{\tau s + 1},
\]

where \( \beta \) and \( \tau \) are the sensitivity and the thermal time constant of the device, respectively. The controller is described by the discrete transfer function

\[
G_2(z) = \frac{c_1 z + c_0}{z + d_0}.
\]

In order to analyze the complete system we need to transform the Laplace representation of the transfer function \( G_1(s') \) into the z-domain. Since the input of the reference sensor is connected to the quantizer, a zero-order hold block can be assumed to exist in between, leading to the transfer function

\[
G_1(z) = \frac{a_0}{z - b_0},
\]

where \( T \) is the sampling time,

\[
a_0 = \beta \left( 1 - \exp\left( \frac{T}{\tau} \right) \right) \quad \text{and} \quad b_0 = \exp\left( \frac{T}{\tau} \right).
\]

The state variable representation of the reference sensor and the controller, shown in Fig. 3, is described by the expression

\[
\begin{bmatrix}
x_k+1 \\ e_k+1
\end{bmatrix} = \begin{bmatrix}
-d_0 & 1 \\ 0 & b_0
\end{bmatrix} \begin{bmatrix}
x_k \\ e_k
\end{bmatrix} + \begin{bmatrix}
0 & 0 \\ (1 - b_0) a_0 & 1
\end{bmatrix} \begin{bmatrix}
q_k \\ r_{k-1}
\end{bmatrix},
\]

where \( q \) is the output of the measuring sensor and \( r \) the
squared and delayed output of the quantizer. The input \( u \) of the comparator results as

\[
\begin{align*}
  u_k = \left[ (c_0 - c_1 d_0) \right] \cdot \begin{bmatrix} x_k \cr \tau_k \end{bmatrix}.
\end{align*}
\]  

(6)

Assuming \( T >> \tau \) (\( \tau \) is of the order of 10 ms and \( T \) in the microsecond range), we can derive the shape of the trajectory in the phase diagram from eqn. (5). It is given by

\[
x_k = A \cdot e^k + B,
\]  

(7)

where \( B \) is defined by the transient behavior of the feedback system and

\[
A = \frac{1}{2b_0 - (q_k \cdot (1 - a_0) - a_0'k)}.
\]  

(8)

The amplitude of the signal \( r_k \) is either 0 or \( r^2 \) since it is obtained from the quantizer. In order to ensure proper working conditions the average duty cycle of the bitstream has to be around the optimal value of 50\% which leads to the condition

\[
A \mid_{r_k = r} = -A \mid_{r_k = 0}.
\]  

(9)

Using eqns. (4), (8) and (9) we obtain the relation

\[
\tau(q_k) = \frac{2 \cdot q_k}{\sqrt{\beta}},
\]  

(10)

which allows us to determine the proper reference voltage for the quantizer under any operating conditions.

We can optimize the noise shaping function of the system by properly choosing parameters \( c_0, c_1 \) and \( d_0 \) in the controller \( G(z) \). The phase diagram representation of eqn. (5) is divided into two parts by the quantizer, one where \( r = 0 \) and the other where \( r = r^2 \). The equation of the straight line that separates these two parts of the phase diagram can be derived from eqn. (6) and is given by

\[
e_k = \frac{c_1 d_0 - c_0}{c_1} \cdot x_k.
\]  

(11)

Since the system contains a delay after the quantizer, we have to provide a finite slope to the line to ensure the stability of the system. Fig. 4 and Fig. 5 show the phase diagram and the spectrum of the bitstream for two different slopes. One can observe, that the behavior of the system improves as the absolute value of the slope decreases. We obtained optimal performances using \( c_1 = 1.5, c_0 = -1 \) and \( d_0 = -1 \) (slope = -1/3). Moreover, we observed that further reduction of the absolute value of the slope does not improve the behavior of the system because of the inherent quantization error. The results were obtained by MATLAB simulations of the complete system shown in Fig. 2.

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Fig. 4 - Phase diagram and spectrum of the bitstream with \( c_1 = 2, c_0 = -1 \) and \( d_0 = -1 \) (slope = -1/2)

Fig. 5 - Phase diagram and spectrum of the bitstream with \( c_1 = 1.5, c_0 = -1 \) and \( d_0 = -1 \) (slope = -1/3)
IMPLEMENTATION

We implemented the interface circuit using the switched capacitor technique together with a fully differential architecture, as shown in Fig. 6. The sensor signal is sampled during clock phase $\Phi_1$ and integrated into capacitors $C_{1P}$ and $C_{1N}$. The charge stored in $C_{1P}$ and $C_{1N}$ at the end of phase $\Phi_1$ is given by

$$V_{out1}C_1 = V_{out2}C_1z^{-1} + V_{in2}[C_{inz}z^{-1} - C_{inz} - C_{inz}]$$

where $C_{1P}$, $C_{1N}$ and $C_{inz}$ denote the capacitance values of $C_{1P}$, $C_{1N}$, $C_{inz}$ and $C_{inz}$, respectively. The resulting transfer function in the z-domain is

$$G_2(z) = \frac{V_{out1}}{V_{in2}} = -\frac{z(C_{inzC} + C_{inzZ}) - C_{inz}}{C_1(z-1)}.$$  

Choosing $C_1 = C_{inz} = 1 \text{ pF}$ and $C_{inz} = 0.5 \text{ pF}$ we obtain the desired transfer function

$$G_2(z) = \frac{1.5z - 1}{z-1}.$$  

During phase $\Phi_2$, $V_{out}$ is held on capacitor $C_H$ and the comparator is latched. The resulting digital signal is fed back to the reference sensor through the circuit shown in Fig. 7. It is a low on-resistance, high current driving capability switch implemented using a local feedback loop with an additional operational amplifier. The switch is driven by the bitstream that is returned to zero with phase $\Phi_1$. A dummy heating resistor was introduced in order to ensure the reference voltage is available during both clock phases. It can be observed that the signal supplied to the incremental A/D converter corresponds exactly to the reference voltage despite non-idealities.

The complete system, including the sensor and the incremental A/D converter, was integrated in the 2 $\mu$m CMOS process. Fig. 8 shows the layout of the interface circuit. To reduce the size of the sensor and the reference, both structures were placed on the same membrane. The thermal cross talk does somewhat affect the signal to noise ratio S/N of the sensor and slightly reduces sensitivity $B$. Both effects were carefully investigated by finite element analysis [5] and the system was optimized to keep these drawbacks to an acceptable limit.

CONCLUSIONS

In this paper we proposed a novel system architecture for an AC-power sensor. The dynamic range of the system was optimized and the required die size was minimized by placing both the sensor and the reference structure on the same membrane. We proved the stability and optimized the performance of the proposed system by non-linear analysis. The complete system, including the sensor, was integrated in a 2 $\mu$m CMOS process.

REFERENCES


