DIGITALLY-PROGRAMMABLE AND PERSONALIZABLE
CMOS HEARING AID CIRCUIT

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ABSTRACT
A CMOS mixed-mode fully-differential signal processor, that constitutes the core of a hearing aid system, is introduced in this paper. The circuit is fully and remotely controllable by means of dual-tone multifrequency (DTMF) encoded tones, transmitted by an external unit. A general description of the whole system is provided, and the implementations of some outstanding parts are covered in more detail. The circuit has been fabricated in 1.2 μm CMOS n-well process. It operates from a single 1.3-V battery, consumes typically less than 1 mA and occupies 28 mm² of silicon. Experimental results of the described parts are also reported.

I. INTRODUCTION
The high degree of maturity reached by IC technology in the last years, is allowing the development of new applications and options of electronic devices based on monolithic circuits. In this sense, hearing aids (HA's), indeed, do not constitute any exception [1, 2]. In this paper, a custom CMOS circuit [3], which is the core of a HA system, is presented. The circuit is digitally and remotely programmed to compensate for any particular hearing losses. As information carriers, encoded dual-tone multifrequency (DTMF) signals, transmitted by a remote control unit, are used. The circuit realizes a truly fully-differential (FD) signal processing, which improving the dynamic range and power supply rejection.

II. OPERATION OF THE HEARING AID CIRCUIT
Fig. 1 shows the block diagram (main blocks) of the circuit. Firstly, the level of the signal provided by the input transducer (microphone or inductive coil), is increased by a micropower low-noise preamplifier. A differential-output topology has been chosen for the preamplifier, which allows differential signal processing to be performed by the following stages with no need for "ad hoc" single-ended to double-ended conversion structures. The preamplifier is based on the current-series feedback technique [4], and provides a gain of 24 dB in the audio frequency range keeping total harmonic distortion (THD) smaller than -42 dB with a 1-Vp 1-kHz output signal. As the filter section is based on sampled-data circuits, a third-order MOSFET-C low-pass (LP) filter is used to avoid the aliasing effect inherent to any time discrete circuit. A simple on-chip automatic tuning section controls the cutoff frequency around
8 kHz. Following, an automatic gain control (AGC) circuit with programmable knee point, delivers its output signal to a filter-amplifier section that provides the required frequency response compensation to the hearing-impaired person. This filter section consists of a high-pass (HP) switched-capacitor (SC) filter cascaded with a SC bump equalizer (BE). Finally, a digitally adjustable output amplifier based on pulse-width modulation, drives the HA earphone. A DTMF receiver/decoder in VERDI, by detecting if a valid DTMF command has been transmitted by the remote control unit, acts as volume control and as programmable interface receiver. So, acting as volume control receiver [6], it allows the HA volume to be increased and decreased up to 14 dB of additional amplification, in steps of 2 dB over a determined amplification level which is also programmable. Moreover, acting as programmable interface receiver, this section allows the complete HA characteristics (compression level, frequency response and amplification level) to be chosen among four preprogrammed settings suitable for very different listening situations, which are stored in the remote control unit. The remote control unit is programmed by the audiologist with the help of a PC program. This specifically tailored fitting routine determines, given a particular hearing loss and the transfer function of the HA blocks, the optimum programing set of bits, that are then stored in the commercial EEPROM cells existing into the remote control unit. The circuit is supplied from a single 1.3-V battery, although a DC/DC converter provides a total supply voltage of ±1.5 V to the rest of the blocks, except for a 200-kHz crystal oscillator that operates directly supplied from the battery.

III. AUTOMATIC GAIN CONTROL (AGC) CIRCUIT

In order to avoid disagreeable switching noise in the HA, a gain controlled amplifier implementation with continuous time regulation has been chosen. Fig. 2 illustrates the circuit schematic of the AGC designed. The operation principle is as follows. First of all, a FB common-mode adapter [6], based on a fully-differential difference amplifier, is used to adapt the CM component of the balanced input signals to the input range of the gain controlled amplifier. The outputs \( V_{\text{out}^+} \) and \( V_{\text{out}^-} \) of the gain controlled amplifier (enclosed within the dashed line), are applied to two differential-difference comparators (DDC). These DDC’s along with a NOR gate and a LP filter, constituted by the output resistance of the inverter (MU-MD) and an external capacitor \( C_{\text{in}} \), provide a dc signal. The value of this dc signal is proportional to the time intervals where \( |V_{\text{out}^+}-V_{\text{out}^-}| \) is larger than the programmable AGC compression level \( V_{\text{cr}} \). The transistor driven by the filter output will draw as more current I as higher the duty cycle is, thus decreasing in this manner the control voltage \( V_{\text{c}} \) and, hence, the amplifier gain. The AGC gain is given by \( (V_{\text{in}}-V_{\text{c}})/(V_{\text{in}}-V_{\text{cr}}) \), assuming every MOS resistor with the same (W/L) ratio. Notice that when no compression exists \( (|V_{\text{out}^+}-V_{\text{out}^-}| \) always smaller than \( V_{\text{cr}} \), no current I flows and the gain is automatically tuned to one, since \( V_{\text{c}}=V_{\text{cr}} \) without the need of incorporating any tuning loop to guarantee such condition. The difference between the AGC time constants (attack and release times) is adjusted through the aspect ratios of transistors MU and MD. Fig. 3 shows the experimental AGC static behavior for different compression voltage level \( V_{\text{cr}} \), which is programmed by means of a 4-bit resistor-ladder DAC. The experimental AGC dynamic behavior is illustrated in Fig. 4, where the responses to a sudden increase (attack behavior) and decrease (release behavior) in the input signal, respectively, are shown.

IV. FREQUENCY RESPONSE CORRECTION SECTION

A cascade composed by a second-order HP filter followed by a second-order BE [7], provides the hearing impaired with the relative compensation of his (her) hearing losses. Due to the superior performance of sampled-data filters over other techniques in the audio frequency range, a FD SC digitally-programmable implementation for both structures has been chosen. Each magnitude (cutoff frequency and Q factor of the HP filter, as well as central frequency, peak gain and bandwidth of the BE) is programmed by 3 bits. Thus, the complete filter-
amplifier section has enough flexibility to provide a reasonably accurate compensation for most hearing losses without a very arbitrary shape. Fig. 5 only illustrates the experimental results about the BE bandwidth programmability. The sampling frequency is 50 kHz.

V. CLASS D OUTPUT AMPLIFIER

The load device of a hearing aid system (i.e. the earphone) has a low-pass frequency response and therefore, the final amplification stage can be realized using a class D topology [1]. We have designed a class D amplifier particularly suitable for this application, to minimize power consumption when no input signal is applied. Moreover, we have provided the amplifier with easy gain programmability. The amplifier block diagram is shown in Fig. 6. A high-frequency saw-tooth waveform is compared with the analog differential input signal. The resulting digital waveforms C1 and C2 are processed by the control logic, which generates the driving signals for the switches and the current generators of the output stage (A1 and A2). When the differential input signal (V_{IN} - V_{IN'}) is positive (negative), the switch and the current source driven by A1 (A2) are turned on and the current flows through the load from R to L (L to R). The average current flowing through the load is proportional to the value of the differential input signal, taking into account also the signal polarity. Fig. 7 shows the experimental responses of the amplifier to dc differential input voltages equal to +1 V and -1 V respectively. The duty cycle modulation of the output current, as well as the opposite polarity obtained in response to positive and negative input voltages can be observed. The frequency of the output waveform is 45 kHz. The dc transfer characteristic of the amplifier for different values of the output stage bias current is plotted in Fig. 8. The gain of the stage (i.e. the slope of the curves) is proportional to such bias current that is programmed by 3 bits. Nominally, no output current is delivered with zero input signal. The measured THD for a 1-V_{pp} 1-kHz input signal was lower than -50 dB.

VI. CONCLUSIONS

A mixed-mode CMOS signal processor that, along with a few discrete components, acts as a hearing aid device with new and sophisticated options, has been presented. The device is fully controllable by a remote control unit. The control signals are DTMF tones duly encoded. The circuit has been fabricated in a standard 1.2-μm process, occupies 28 mm² and draws a current typically less than 1 mA from a 1.3-V battery. Fully-differential signal processing techniques are incorporated, resulting a dynamic range higher than 68 dB.

References

Fig. 1. HA simplified block diagram.

Fig. 2. Programmable AGC circuit

Fig. 3. Experimental AGC static behavior.

Fig. 4. Experimental AGC dynamic behavior. Top trace: attack response (vertical: 200 mV/div, horizontal: 8 ms/div). Bottom trace: release response (vertical: 200 mV/div, horizontal: 20 ms/div).

Fig. 5. BE bandwidth programmability.

Fig. 6. Block diagram of class D output amplifier.

Fig. 7. Responses to dc input voltages ($R_c=1$ kOhm).

Fig. 8. Class D amplifier transfer characteristic.