RAISED COSINE WAVEFORM SHAPER FOR GSM BASE STATION

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Abstract: An integrated circuit for a GSM system is described which acts as a raised cosine shaper for the ramp up and ramp down of a transmitted burst. By use of this shaper, GSM specifications for switching transient spectrum and power level versus time are fully met. The circuit which includes two 8 bit D/A converters, was fabricated using a 2 μm CMOS process and its size is about 3*2.8 mm².

1. Introduction

The shape of the "on" and "off" phases of a transmitted burst in a GSM system mainly influences the switching transient spectrum and the transmitted level versus time at the output of the transmitter (TX) modulator. Both these parameters must fulfill the masks and the limits defined in the GSM ETSI specifications (section 05.05) for radio transmission and reception. To reach this target and maintain a reasonable operational margin, a raised cosine was chosen. In fact, by properly tuning the roll-off factor of the raised cosine waveform, the contribution by high frequency harmonic components can be reduced. Thus raised cosine shaper designed is now being incorporated into a fully integrated GSM transmission interface.

![Fig. 1 - Schematic Diagram of the GSM Transmitter.](image1)

![Fig. 2 - Schematic Diagram of the Waveform Shaper.](image2)
2. System and Circuit Description

For optimum transmission conditions suitable control of transmitted power is required. Fig. 1 reports the block diagram of the control loop at the TX level showing how the waveform shaper helps to carry out control. In detail, the generated ramp is summed to the detected one with a proper weight factor. It helps to define the control voltage, \( V_c \), of an automatic gain amplifier, AGC, set in the path of in-phase (I) and in-quadrature (Q) components of the signal to be transmitted. DAC1 generates a reference signal for DAC2, proportional to the power level in TX, and DAC2 produces the desired raised cosine waveform, whose digitised samples are stored in an on-chip memory.

Fig. 2 shows the schematic diagram of the Waveform Shaper architecture. It consists of the cascade of two identical current-steering 8-bit DACs. The interface between DAC1 and DAC2 is performed by means of a fixed factor current divider. By carefully choosing the reference current, \( I_{ref1} \), for DAC1 and the division factor, that is \( I_{ref2} \), both converters can guarantee the foreseen speed.

The DAC structure is based on a segmented 6+2 current cell matrix configuration. [1] [2]. The 6 most significant bits are realised with 63 current cells, each having an equivalent weight of 4 LSBs. The currents corresponding to the two remaining least significant bits are generated through two weighted current cells 1 LSB and 2 LSBs. The current of the cells is switched to the dummy load or to the output node to obtain the foreseen analog output current. Conventionally p-channel switches are used to control currents injected towards ground. In our circuit we have instead used n-channel transistors, since this reduces the output glitches, [3].

The local decoding logic is realised using only NOR gates. That approach minimise the output glitches resulting from propagation delays.
A critical point in the design concerns the choice of the reference currents. Speed requirements mandate high levels for the first DAC reference current. Since the output current of the first converter is used as the reference current of the second one, a current divider is necessary to act as interface. Fig. 3 shows the current divider architecture. The requirements are high frequency operation and high linearity into the total input current range.

Extensive simulations show that the optimal attenuation factor is 15, obtained in two steps. The first is a 1:3 n-channel mirror while the second is a 1:5 p-channel one. The n-channel mirror is the most critical of the two and we used a modified Wilson structure to obtain the desired linearity and output impedance.

The resolution obtained is 1% for the whole input current range (200 μA - 1.2 mA).

3. Experimental Results

In order to guarantee compatibility with the existing GSM interface the Waveform Shaper was fabricated using a 2 μm CMOS double-poly, double-metal process. The total area is about 3 x 2.8 mm². Fig. 4 shows the microphotograph of the silicon prototype. The circuit was laid out in order to minimise skew delay between the command phases of the current generators. The silicon prototypes were tested at the nominal working frequency (13 MHz for the first DAC, 1.083 MHz for the second). Fig. 5 shows the raised cosine ramp-down generated for different values of the transmitted power before the filtering stage. As can be seen, the time interval dedicated to ramp-down is identical for all the values of TX power and is also equal to the time dedicated to ramp-up. Fig. 6 shows the DNL obtained from DAC1. The values measured are less than 0.4 LSB. Fig. 7 shows the total DNL of the ramp generator, that means the cascade of DAC1 plus DAC2. This structure exhibits an intrinsic no-linear transfer function as can be seen from the shape of the total DNL. Moreover, the maximum DNL value referred to DAC1 plus DAC2, is below 0.7 LSB as was expected.
Fig. 8 - Total DNL of the ramp generator for a discrete number of the power transmitted.

Fig. 9 shows the total INL, whose maximum value is less than 0.9 LSB. All these values are well within the specifications.

4. Conclusions

This paper has presented a new topology architecture for a Waveform Shaper to be used inside a GSM base station transmitter. It adopts a novel architecture solution using two current switching DACs with a current divider as interface. This corresponds to a current MDAC whose multiplying factor is generated by the other DAC. The experimental results showed the expected resolution both for the single blocks and for the total transmitter. A total DNL and INL as low as 0.7 and 0.9 LSB respectively were measured at nominal working frequency.

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References