WAVEFORM SHAPING FOR GSM SYSTEMS

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ABSTRACT

This paper describes a new integrated topology circuit for a waveform shaper which will be used inside a GSM system. The circuit generates a raised cosine shape output for the ramp up and ramp down of a transmitted burst. The circuit was realised using two 8-bit current-steering digital-to-analog converters. The measured results of the transient spectrum and the power level versus time show that the circuit fully meets GSM specifications.

I. INTRODUCTION

The GSM digital cellular radio system was devised to meet the increasing demand for mobile communication in Europe. GSM provides a new standard for radio mobile communication that overcomes most of the drawbacks of the existing analogue networks. It makes several facilities and services available to subscribers allowing both traditional speech communication and data transmission.

The use of digital techniques also guarantees high immunity to co-channel interference allowing a more efficient reuse of frequency carriers and a larger number of subscribers.

II. THE GSM SYSTEM

The GSM system is based both on the time- and frequency-division multiple-access technique (TDMA-FDMA). It employs a Gaussian minimum shift keying (GMSK) modulation, with a 0.3 modulation index, which is characterised by a narrow band spectrum.

The primary assigned RF bands (P-GSM 900) are in the range of 890-915 MHz for mobile to base station transmission (up-link) and in the range of 935-960 MHz for base station to mobile transmission (down-link).

In these bands 124 radio frequency carriers are available with 200 kHz spacing. There are 8 time-division physical channels associated to each channel. Each having a time slot of about 577 µs assigned to it, with a frame repetition period of 4.6 ms. The bit period is 3.69 µs.

Furthermore GSM 900 is allowed to operate in an extended band, wider by 10 MHz, in the range of 880-890 MHz for up link and 925-935 for down link (E-GSM 900).

The integrated circuit described here includes a waveform generator which has to supply an optimised shaping over a transmitted burst. The optimisation is to be intended as fulfilling the limits defined in GSM ETSI specifications (Section 05.05) for radio transmission. In particular, the way in which a burst is switched on and off and the corresponding profiles are of main concern for the switching transient spectrum and for the transmitted level versus the time resulting at the output of the transmitter modulator.

In meeting GSM system specifications, while preserving a reasonable margin for operation over the full temperature range and atmospheric stresses, a raised cosine proved to be a suitable waveform shape. By properly choosing the roll-off factor and the period of the raised cosine it is possible to reduce the contribution of high frequency harmonic components, respecting the ramp up and ramp down masks specified for a time slot at the same time.

III. SYSTEM DESCRIPTION

In the transmission direction TX, the system is designed to operate in a closed loop configuration. The effect of this choice is to control the transmitted power both as regards the rising and the falling profiles and the nominal value. The block diagram of the control loop in TX is shown in Fig. 1. Referring to Fig. 1, it is easy to derive that the loop is closed by means of the control voltage, $V_C$, for the AGC. In detail, $V_C$ is obtained by combining the ramp detected from the signal to be transmitted and the ramp generated by the waveform shaper with proper weight factors.

Fig. 1. GSM System Architecture.
With good approximation the AGC transfer function can be considered as linear. Therefore, to impose the raised cosine shape on the generated ramp it is enough to obtain the desired characteristics of Pout.

IV. WAVEFORM SHAPER ARCHITECTURE

Fig. 2 shows the schematic diagram of the Waveform Shaper architecture. It consists of the cascade of two identical current-steering 8-bit DACs. The interface between DAC1 and DAC2 is performed by means of a fixed factor current divider. By properly choosing the reference current, \( I_{\text{ref1}} \), for DAC1 and the division factor, meaning \( I_{\text{ref2}} \), both converters can guarantee the foreseen speed.

V. BASIC BLOCKS AND LAYOUT

Fig. 3 shows the schematic diagram of the DAC architecture. The structure is based on a segmented 6+2 current cell matrix configuration. The 6 MSB significant bits are realised with 63 equal current cells, each having an equivalent weight of 4 LSBs. The currents corresponding to the remaining two least significant bits are generated through two weighted current cells of 1 LSB and 2 LSBs respectively.

To obtain the corresponding analog output current all the cell currents are summed together at the output node of the circuit according to the digital input. Fig. 4 shows the schematic diagram of the circuit used to generate the two complementary currents of each elementary cell used in the matrix. Each current source transistor (M1 - M4) has an elementary current corresponding to 1 LSB. The W/L aspect ratio used minimises mismatch errors between the cells. The two binary weighted cells at 1 and 2 LSBs, are obtained by subtracting 3 and 2 current source transistors respectively from the elementary cell of the matrix.

Fig. 5 shows the schematic diagram of the local decoder. To minimise the output glitches resulting from propagation delays, the local decoder contained inside each current cell is realised using only NOR gates. To obtain a digital delay as in the 4 LSB current cells, a delay equaliser is used to drive the two weighted current-cells of the DAC corresponding to the 2 LSBs.

Conventionally p-channel switches are used to control currents injected toward ground. In our circuit we have, instead, used n-channel transistors, since this reduces the
output glitches, [3].

A critical point in the design concerns the choice of the reference current. Speed requirements mandate high value for the first DAC reference current. Since the output current of the first converter is used as the reference current of the second one, a current divider is necessary as an interface. Fig. 6 shows the current divider architecture. The requirements are high frequency operation and high linearity for the whole input current range. Extensive simulations show that the optimum attenuation factor is 15 obtained into two steps. The first is an 1:3 n-channel mirror while the second is an 1:5 p-channel mirror. The n-channel mirror is the most critical of the two and we used a modified Wilson structure to obtain the desired linearity and output impedance.

The resolution obtained is 1% for the whole input current range (200 mA - 1.2 mA). The Waveform Shaper was fabricated using a 2 μm CMOS double-poly, double-metal process. The total area is about 3*2.8 mm². Fig. 7 shows the microphotograph of the silicon prototype. The circuit was laid out in order to minimize skew delay between command phases of the current generators.

VI. EXPERIMENTAL RESULTS

The silicon prototypes were tested at the nominal working frequencies (13 MHz for the first DAC, 1.083 MHz for the second). Experimental measurements were in good agreement with the expected results. Fig. 8 shows the generated raised cosine ramp-down for different values of the transmitted power before the filtering stage. As can be seen the time interval dedicated to ramp-down is identical for all the values of TX power and it is also equal to the time dedicated to ramp-up.

Fig. 8. Generated raised cosine (different transmitted powers) before the filter.

Fig. 9. DNL of DAC1.

Fig. 10. INL of the single D/A converter.
Fig. 11. Switching transient spectrum for the transmission of 8 time slot at maximum power.

Fig. 9 shows DNL error obtained from tests performed on the single DAC with automatic test equipment (LTX). The maximum measured value is quite good, lower than ±0.2 LSB. The maximum measured integral non linearity value is lower than ±0.5 LSB, see Fig. 10. Measurements of the power glitch compared with a standard switch topology have shown a 70% power reduction.

To test the capability of the waveform shaper IC several experimental measurements were performed at system level. The shaper was used to drive a transmitter equipment under normal transmission GSM traffic channels. In Fig. 11, the switching transient spectrum is shown for the transmission of 8 time slots at maximum power, to enhance the intrinsic effect of the switching operation.

As can be seen, at 400 kHz away from the carrier, the attenuation is well below the limits of GSM specifications (-57 dBc). Fig. 12 shows the ramp up and the ramp down profiles of a transmitted time slot for the same conditions. The curves fully satisfy the GSM masks.

V. CONCLUSION

This paper has presented a new topology architecture for a Waveform Shaper to be used inside a GSM base station transmitter. It uses a novel architecture solution using two current switching DACs with a current divider as interface. This corresponds to a current MDAC with the multiplying factor being generated by the other DAC. The experimental results gave the expected resolution both for the single blocks and the total transmitter. A total DNL and INL as low as 0.2 and 0.5 LSB respectively were measured at the nominal working frequencies. The shaper was also used to drive transmitter equipment under normal transmission condition, GSM traffic channels. The switching transient spectrum obtained is well below the limits set by GSM specifications and fully satisfies the GSM masks.

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REFERENCES


