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40 MHz IF 1 MHz Bandwidth Two-Path Bandpass $\Sigma\Delta$ Modulator With 72 dB DR Consuming 16 mW

Ivano Galdi, Student Member, IEEE, Edoardo Bonizzoni, Member, IEEE, Piero Malcovati, Senior Member, IEEE, Gabriele Manganaro, Senior Member, IEEE, and Franco Maloberti, Fellow, IEEE

Abstract—A bandpass $\Sigma\Delta$ modulator with two time-interleaved second-order modulators and cross-coupled paths is described. Split zeros around the 40 MHz IF provide a signal band of 1 MHz with 72 dB DR and 65.1 dB peak SNR. The circuit, integrated in a 0.18 $\mu$m CMOS technology, uses a 60 MHz clock per channel. Experimental results show that the in-band region is not affected by tones caused by mismatches and that a two-tones input causes an IMD signal of 68 dBc. The power consumption is 16 mW with 1.8 V supply.

Index Terms—Analog–digital conversion, CMOS integrated circuits, sigma-delta modulation.

I. INTRODUCTION

The architecture of portable communication systems often includes $\Sigma\Delta$ bandpass analog-to-digital converters (ADCs) [1], because their low power enables the direct conversion of the intermediate frequency (IF) signal [2]. They replace equivalent Nyquist-rate converters with a large sampling rate that, although allowing the placement of the IF anywhere in the Nyquist interval, require a power that would be excessive for portable applications [3].

$\Sigma\Delta$ bandpass ADCs achieve low power, medium-high dynamic range (68–72 dB) and relatively wide signal bandwidth (1–2 MHz) that, for some applications, relaxes the demands on the digital filter used after the modulator. There are several ways to achieve a bandpass transfer function in a $\Sigma\Delta$ modulator. The most straightforward approach is the use of resonators instead of integrators in the modulator loop. This solution, however, requires the use of a loop filter with order $2L$ to achieve $L$th order noise shaping, thus introducing stability issues. Another approach to obtain the ($N\cdot L$)th-order bandpass $\Sigma\Delta$ modulator is the use of time-interleaved structures realized with $N$ parallel paths with $L$th-order low-pass transfer function, each operated with a clock frequency equal to $f_s/N$, $f_s$ being the sampling frequency of the complete ADC. This solution leads to a bandpass response centered at $f_s/N$ without introducing stability issues, but suffers from spurious tones placed around integer multiples of $f_s/N$ (i.e., in the useful band of the modulator), due to the offset, gain, and timing mismatches among the paths.

As a tradeoff between circuit complexity, power consumption and sampling frequency, a $\Sigma\Delta$ modulator using a two-path bandpass architecture with a 4-bit quantizer is here proposed. The use of a novel noise transfer function (NTF) synthesis technique, based on cross-coupled branches in the time-interleaved structure, allows us choosing a value different from $f_s/N$ for the center frequency of the bandpass modulator, thus eliminating the above mentioned issue related to in-band tones caused by mismatches. Indeed, the experimental results show a tone free spectrum with a flat low-noise region of ±1 MHz around 40 MHz (less than 125 nV/$\sqrt{Hz}$ with a ±1 V differential reference). With 1 MHz signal band, the dynamic range is 72 dBFS (peak SNR = 65.1 dB). With 2 MHz signal band the above metrics worsen by 4 dB. The sampling frequency $f_s$ is 120 MHz. Since we use a two-path architecture, the operating frequency of each path is 60 MHz, which equals the Nyquist frequency, $f_N$. Thanks to the proposed NTF synthesis technique, the bandpass response is centered around $1/3f_s$ and $2/3f_s$ (i.e., in a region of the spectrum which is free of spurious tones introduced by the mismatches). The power consumption is 16 mW with 1.8 V supply.

II. NTF SYNTHESIS

As mentioned above, bandpass $\Sigma\Delta$ modulators using an $N$-path architecture suffer from tones in the signal band caused by path mismatches. Moreover, the $N$-path architecture inherently produces NTF zeros distributed around the unity circle. The zeros out of the signal band (centered around $f_s/N$) negatively affect the gain and reduce the noise shaping benefits [4]. The proposed approach for the synthesis of the NTF overcomes the above limits. The IF is far away from $f_s/N$ and the NTF contains only the necessary zeros. The proposed synthesis techniques starts with an $N$-path scheme whose NTF has the desired order (i.e., the same highest order term in $z^{-1}$ as the desired NTF). The missing terms appearing from the difference between desired and initial NTF are achieved by additional branches introduced in the architecture.

A. Synthesis of NTF: $1 + \alpha z^{-1} + z^{-2}$

The basis for a bandpass response design is the second-order transfer function

$$NTF = 1 + \alpha z^{-1} + z^{-2}. \quad (1)$$

When $\alpha = 0$, the NTF zeros are at $\pm j$, while when $\alpha = 1$, the NTF has zeros at $1/3f_s$ and $2/3f_s$. The two-path architecture of Fig. 1 uses a $z^{-2}/(1 + z^{-2})$ loop transfer function, thus enabling a $z \rightarrow z^2$ transformation, [4], but the two-period
delay is distributed before and after the quantizer. Therefore, the uncorrelated quantization noises, $\varepsilon_1$ and $\varepsilon_2$ in the two paths, are available one clock period after the input injection. Since a two-path plain scheme that uses a pseudo-integrator $z^{-1}/(1 + z^{-2})$ gives rise to $\text{NTF} = 1 + z^{-2}$, the missing term is $\alpha z^{-1}$. The cross-coupled injections of $\varepsilon_1$ and $\varepsilon_2$ multiplied by $\alpha$ provide the result. The missing term for each path shows up on the other path, but the combination obtained by the time inter-leaving of $y_1$ and $y_2$ gives rise to

$$y = x \cdot z^{-1} + \frac{\sqrt{\varepsilon_1^2 + \varepsilon_2^2}}{2} (1 + \alpha z^{-1} + z^{-2})$$

(2)

which accounts for the quadratic superposition of the quantization noise and the interpolation by two at the output.

B. Synthesis of $\text{NTF} = (1 + \alpha_1 z^{-1} + z^{-2})(1 + \alpha_2 z^{-1} + z^{-2})$

This design uses a NTF equal to $(1 + \alpha_1 z^{-1} + z^{-2})(1 + \alpha_2 z^{-1} + z^{-2})$ for an effective noise shaping. Indeed, even a fourth-order NTF equal to $(1 + \alpha_1 z^{-1} + z^{-2})^2$ enhances the noise reduction around $1/3f_n$ and $2/3f_n$, but having two zeros at the same frequency is appropriate for small signal band (and large oversampling ratio, OSR). On the contrary, when the OSR is low, it is more convenient to split the zeros and allow the shaping between them to rise up to a level that does not degrade the SNR, as conceptually shown in Fig. 2. We then chose a fourth-order modulator because, with multi-bit quantization, this is optimal for an SNR better than 70 dB, 2 MHz signal bandwidth centered around 40 MHz IF and a clock frequency of 120 MHz.

The synthesis of $\text{NTF} = (1 + \alpha z^{-1} + z^{-2})^2$ will be considered below, while the zeros splitting, achieved by exploiting the finite gain of the operational amplifiers, will be discussed afterwards. Let us consider a two-path time interleaved structure. If this is based on pseudo-integrators with transfer function $z^{-1}/(1 + z^{-1})$ and $1/(1 + z^{-1})$, after the $z^{-1} \rightarrow z^{-2}$ transformation the NTF will become $(1 + z^{-2})^2$, which is the core term used for the synthesis. The desired NTF can then be expressed as

$$\text{NTF} = (1 + \alpha z^{-1} + z^{-2})$$

$$= 1 + \alpha z^{-1} + z^{-2} + \alpha z^{-1} + \alpha^2 z^{-2} + \alpha z^{-3} + z^{-2} + \alpha z^{-3} + z^{-4}$$

$$= [(1 + z^{-2})^2 + \alpha^2 z^{-2}] + z^{-1} [2\alpha(1 + z^{-2})].$$

(3)
This contains the core and missing terms. Equation (3) contains two parts, in square brackets, both function of $z^{-2}$. Therefore, the implementation of those terms can be obtained with a $z^{-1} \rightarrow z^{-2}$ transformation. Moreover, the second part needs a single clock delay.

Since a two-path time-interleaved scheme implies the $z^{-1} \rightarrow z^{-2}$ transformation, it is necessary to introduce the $+\alpha^2 z^{-1}$ missing term on to the core to obtain $(1 + z^{-1})^2 + \alpha^2 z^{-1}$. The scheme of Fig. 3 achieves this objective. The architecture is a second order modulator, with $1/(1 + z^{-1})$ blocks and an extra feedback that injects $\alpha^2$ times the quantization noise at the input of the modulator. It is known that the quantization noise is obtained from the subtraction of input and output of the quantizer. The scheme of Fig. 3 combines the quantization part with the conventional feedback term. The use of the block of Fig. 3 in a two-path time interleaved scheme, as shown in Fig. 4, synthesizes the first part of the NTF.

To second part of (3) requires a $z^{-1}$ delay that is introduced by the time-interleaved operation. Moreover, the transfer function from the input of the second pseudo-integrator to the output is $(1 + z^{-1})$ that, after the $z^{-1} \rightarrow z^{-2}$ transformation, becomes $(1 + z^{-2})$. Therefore, cross-coupling paths of the quantization errors weighted by $2\alpha$ realize the second part of (3).

The diagram of Fig. 5, which shows the complete single path architecture, allows any zeros placement (with $\alpha = 1$ there are pairs at $1/3f_s$ and $2/3f_s$). The capacitance used in the cross coupled path determines the value of $2\alpha$.

The complete block diagram of the proposed modulator is shown in Fig. 6. The interpolation of the two paths is the output, a signal sampled at twice the clock frequency used in each path. A possible offset mismatch of the used opamps gives rise to a square wave with $f_s/2$ frequency while a gain mismatch $\beta$ is equivalent to the multiplication of even samples by $1 + \beta/2$ and odd samples by $1 - \beta/2$ [5]. Therefore, the gain mismatch causes a square wave modulation of the input at $f_s/2$ with amplitude $\beta$. Since the signal is around $f_s/3$, the modulation tones fall at $f_s/6$. Therefore, the tones caused by mismatch are away from the signal band. The cross-coupled connections required to inject the second term of the NTF create a loop whose effect can be studied in the time domain. A possible DC signal caused by the offset mismatch of the second opamps introduces a tone at $f_s/4$. An error in the cross-
coupling coefficients caused by capacitor mismatch moves the NTF zeros. The shift keeps the zeros on the unity circle if they are suitably apart. Moreover, the shift is negligible if the matching is better than 0.4%.
The circuit implementation of the transfer function \(1/(1+z^{-1})\) or \(z^{-1}/(1+z^{-1})\) requires an inversion of the previous output every clock period. The same result can be obtained by modulating by \(\pm1\) at \(f_c/2\) both input and output of a conventional integrator [4], [6]. The scheme reported in Fig. 7 realizes the \(\pm1\) modulation at half of the clock frequency at input and output of an inverting or noninverting integrator. Indeed, since the square wave modulation at the output of the first integrator and one at the input of the next integrator cancel one another, the architecture requires the \(\pm1\) switches only at input and output of the entire scheme and in the cross-coupled branches.

Since the first and second integrator opamps in the first and in the second path operate during different phases with a \(z^{-1}\) delay, it is possible to use only one opamp for both phases (opamp sharing). The opamp is assigned to one path during one phase and to the other path during the other phase. This choice saves power [7] and ensures the same offset in the two paths. The architecture is robust against offset mismatch because the associated tone is far away from the signal band. However, it is important to keep the offset low to avoid dynamic range limitations. To obtain opamp sharing the integrating capacitors of each path are disconnected from the opamp output with a switch when the opamp is used for the other path. Using a single opamp on both phases demands for higher bandwidth and slewing. Nevertheless, transistor-level simulations show that, overall, using a single opamp with this increased dynamic performance still requires over 35% less power than simultaneously using two independent opamps with the more relaxed performance, one for each of the two paths. Since each path uses equal networks at the input and in the opamp feedback, the required specifications are the same for the two phases.

The opamps of the first and of the second integrator have the same architecture, but use different bias currents, consistently with the different slew-rate and feedback factors. They are class-AB fully-differential mirrored cascode amplifiers, with switched capacitor common-mode feedback (not shown). The simplified schematic diagram is shown in Fig. 8. The mirror elements \(M_{10}\) and \(M_{15}\) provide a scaled replica of the output currents implementing the push-pull operation on the output stage. The bias voltages of the two cascode transistors enable a dynamic output range of \(\pm1\) V differential. The key metrics of the opamps are given in Table I. Notice that the DC gain is relatively low. This is done on purpose, because the effect of the finite gain, also verified by simulations, is to split coincident NTF zeros and move them apart on the unity circle. This is intentionally done to increase the signal band. To explain this effect, it is worthwhile to remember that, as it happens for a conventional integrator, the finite gain of the opamp causes a damping in the response [5]: the finite gain changes the ideal response \(z^{-\gamma}/(1+z^{-1})\) into

\[
T = \frac{(1+\varepsilon_G)z^{-\gamma}}{1+(1+\varepsilon_P)z^{-1}}
\]

(4)

where \(\varepsilon_G\) and \(\varepsilon_P\) denote a gain and a phase error, respectively. The effect on the NTF reported in (3) is given by two leakage terms. The one on \(z^{-4}\) is negligible (the coefficient is almost 1 for a reasonable gain), but the effect on the coefficient of \(z^{-2}\)

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**Table I: OPAMP PERFORMANCE SUMMARY**

<table>
<thead>
<tr>
<th>Feature</th>
<th>First integrator</th>
<th>Second integrator</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>46 dB</td>
<td>42 dB</td>
</tr>
<tr>
<td>Unity gain frequency</td>
<td>200 MHz</td>
<td>250 MHz</td>
</tr>
<tr>
<td>Capacitive load</td>
<td>1 pF</td>
<td>200 fF</td>
</tr>
<tr>
<td>Slew-rate</td>
<td>200 V/\mu s</td>
<td>260 V/\mu s</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.2 mW</td>
<td>2.3 mW</td>
</tr>
</tbody>
</table>
is such that the zeros are split apart. The best is when the zero split and the reduced attenuation of the quantization noise between the zeros is lower than the noise floor corresponding to the desired SNR. With a given number of quantizer's bits \( N \) and a given OSR it is necessary to have

\[
H_N(f_{IF})_{\text{dB}} = \text{SNR} - 6.02 \cdot N - 1.74 - 10 \cdot \log_{10}(\text{OSR})
\]  

(5)

where \( H_N \) is the noise transfer function.

Therefore, with \( N = 4 \), OSR = 30, and a desired SNR = 70 dB, an \( H_N(f_{IF}) \) as shown in Fig. 9 is enough. The attenuation at \( f_{IF} \) is 40 dB.

Conversely, the bandwidth and the slew-rate must be relatively large because of the feedback factor, the cross-coupled paths at the input of the second opamp and the foreseen sharing between the two paths. Simulations at the transistor level show that bandwidths of 200 MHz and 250 MHz and slew rates of 200 V/\( \mu \)s and 260 V/\( \mu \)s are needed for the first and the second opamp, respectively. Correspondingly, 1.2 mW and 2.3 mW are consumed by the first and second opamp, respectively.

A preamplifier with gain of 4 followed by a latch implements the differential to single ended conversion. A conventional double-positive feedback loop realizes the latch.

A single resistive divider of 16 equal 500-\( \Omega \) resistors provides the reference voltages of the two flash ADCs. The input switched capacitor structure, made of 16 unity elements equal to 25 fF, also realizes the DAC function. A custom designed combinatory digital logic performs the required operations well within the clock period of 16.5 ns.

IV. EXPERIMENTAL RESULTS

The proposed modulator was integrated using a 0.18 \( \mu \)m single-poly five-metal CMOS technology. Fig. 11 shows the microphotograph of the chip; the active area is 0.44 mm\(^2\). The reference voltages are external to the circuit and no internal buffer is used. This limits the power consumption, but limits the settling performance due to the ringing induced by bonding inductance of the connection from pin to pad. The duration of the ringing limits the usable clock frequency that, for a TQFP package, is about 16 MHz per path equivalent to an IF of 10.7 MHz. The use of an LLP (also known as a QFN) package, whose bonding inductance is dramatically lower than the TQFP, allows the use of the 60 MHz clock with IF 40 MHz. The consumed power depends on the clock frequency. With 16 MHz it is 10.5 mW, while with 60 MHz the increased band and slewing required for the opamps leads to 16 mW.

Fig. 12 shows the measured output spectrum. The in-band noise is almost flat over the used range with a floor equal to
The performance of the modulator is summarized in Table III. Since the IF and the bandwidth scale down with the clock frequency, the circuit can meet various specifications. For example, digitizing AM/FM radio broadcasting signal requires

125 nV/√Hz which is enough to achieve the desired SNR. The spectrum shows a tone at $f_N/2$ with amplitude equal to $-34$ dB.

It is caused, as described above, by a mismatch between the two paths. The amplitude (20 mV) slightly reduces the full scale of the modulator, that, however, is mainly limited by the quantization noise.

Fig. 13 shows the SNR as a function of the input amplitude for three different bandwidths 1 MHz ($\pm 0.5$ MHz), 2 MHz ($\pm 1$ MHz) and 4 MHz ($\pm 2$ MHz). Since there are no in-band tones, the SNDR is equal to the SNR. Because of the flat noise floor, the SNR increases as the inverse of the square root of the oversampling ratio up to a bandwidth of $\pm 1.5$ MHz. The peak SNR occurs around $6$ dB even if the circuit uses a 4-bit quantizer. The limit, predicted by behavioral simulations, is due to the processing of the two quantization errors and the gain used to implement the missing terms. It is worth pointing out that in the presented modulator the position of the noise-shaping zeros is fixed for any considered bandwidths. Notice that, from Fig. 13, for 1 MHz band, the SNR occurs at $72$ dB and, according to one of the used definitions, it represents the dynamic range (DR).

The power efficiency of data converters is often assessed with a figure of merit, defined as $\text{FoM} = P/(2^{\text{ENoB}} \cdot 2 \cdot \text{BW})$. However, this definition is more suitable to low-pass responses, while, understandably, having the input signal at the IF frequency requires more power [8]. For this, we propose the following FoM for a bandpass converter:

$$\text{FoM}_{\text{BP}} = \frac{P}{2^{\text{ENoB}} \cdot 2 \cdot \text{BW} \left(1 + 3 \cdot \frac{\text{IF}}{f_N}\right)}$$

which would lead, for the proposed modulator, to a $\text{FoM}_{\text{BP}} = 1.11$ pJ/conv-lev. A comparison with previously reported bandpass $\Delta \Sigma$ modulators is given in Table II.

The two-tone intermodulation (IMD) test ($f_1 = 40.274$ MHz, $f_2 = 39.874$ MHz) quantifies the linearity of the circuit. An amplitude of the two tones at $-14$ dB (as shown in Fig. 14) leads to an intermodulation product at $f_2 - f_1$ of about $-68$ dBc. The result is 3 dB better than what was obtained in [9] using a complex solution that requires four times more power.

The performance of the modulator is summarized in Table III. Since the IF and the bandwidth scale down with the clock frequency, the circuit can meet various specifications. For example, digitizing AM/FM radio broadcasting signal requires

<table>
<thead>
<tr>
<th>Feature</th>
<th>This work [10]</th>
<th>[4]</th>
<th>[9]</th>
<th>[11]</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power [mW]</td>
<td>16</td>
<td>150</td>
<td>88</td>
<td>30</td>
<td>37</td>
<td>47.5</td>
<td>12</td>
</tr>
<tr>
<td>ENoB</td>
<td>10.52</td>
<td>11.16</td>
<td>11.5</td>
<td>8.67</td>
<td>11.66</td>
<td>12.99</td>
<td>6.73</td>
</tr>
<tr>
<td>Peak SNDR [dB]</td>
<td>65.1</td>
<td>69</td>
<td>71</td>
<td>54</td>
<td>72</td>
<td>80</td>
<td>42.3</td>
</tr>
<tr>
<td>Bandwidth [MHz]</td>
<td>1</td>
<td>2.5</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.27</td>
<td>0.2</td>
</tr>
<tr>
<td>IF [MHz]</td>
<td>40</td>
<td>40</td>
<td>10.7</td>
<td>47.3</td>
<td>60</td>
<td>23</td>
<td>10.7</td>
</tr>
<tr>
<td>$f_s$ [MHz]</td>
<td>60</td>
<td>60</td>
<td>18.525</td>
<td>94.6</td>
<td>120</td>
<td>46</td>
<td>21.4</td>
</tr>
<tr>
<td>FoM [pJ/conv-step]</td>
<td>5.44</td>
<td>13</td>
<td>75.9</td>
<td>183</td>
<td>28.4</td>
<td>10.8</td>
<td>282</td>
</tr>
<tr>
<td>FoM$_{\text{BP}}$</td>
<td>1.8</td>
<td>4.34</td>
<td>27.8</td>
<td>73.3</td>
<td>11.4</td>
<td>4.3</td>
<td>113</td>
</tr>
</tbody>
</table>
only 10.5 mW, while obtaining 67 dB peak SNR and 72 dB DR. For higher IF and band, the power must be increased almost proportionally, thus preserving the FoM_TBP.

V. CONCLUSION

In this paper, a bandpass $\Sigma\Delta$ modulator that uses two time-interleaved second-order modulators and cross-coupled branches, allowing synthesis of a passband that is free of mismatch-induced spurious signals, is described. Split zeros around the 40 MHz IF provide a dynamic range of 72 dBFS, 69 dBFS, and 50 dBFS for signal bands of 1 MHz, 2 MHz, and 4 MHz, respectively (full-scale signal $\pm 1$ VPP differential). The in-band noise floor is about 125 nV/$\sqrt{Hz}$. The circuit, integrated in a 0.18 $\mu$m CMOS technology, uses a 60 MHz clock in each channel. For two tones at $-14$ dB, the intermodulation is about $-68$ dBc. The power consumption is 16 mW with 1.8 V supply and can be decreased to 10.5 mW with 16 MHz clock per channel.

Table III

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_s$</td>
<td>60 MHz (x 2)</td>
</tr>
<tr>
<td>IF</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Voltage References</td>
<td>$\pm 0.5$ V</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>up to 4 MHz</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>65.1 dB @ 1 MHz Band</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.44 mm$^2$</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>16 mW</td>
</tr>
<tr>
<td>IMD</td>
<td>68 dBc</td>
</tr>
<tr>
<td>DR</td>
<td>72 dB @ 1 MHz Band</td>
</tr>
</tbody>
</table>

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REFERENCES


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