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A 107.4 dB SNR Multi-Bit Sigma Delta ADC With 1-PPM THD at -0.12 dB From Full Scale Input

Jian-Yi Wu, Zhenyong Zhang, Rajaram Subramoniam, and Franco Maloberti, *Fellow, IEEE*

Abstract—A second order sigma delta modulator (SDM) with a 5-bit quantizer has been presented using several novel techniques: simplified DAC arrays for easy implementation, high-order truncation noise shaping for increased tolerance to analog imperfections, and an extended dynamic range for a maximum input signal swing of up to -0.12 dB_{FS} (Full Scale). With truncation filters and a pseudo SDM in the DSP, the truncation and saturation errors are compensated through the DAC arrays and the DSP. The design, fabricated in a $0.18\text{ }\mu\text{m}$ dual gate oxide (DGO) process obtains a signal-to-noise-and-distortion ratio (SNDR) of 105.9 dB and a dynamic range (DR) of 107.4 dB with 31.25-KHz bandwidth at an 8-MHz sampling frequency and a power consumption of 14.7 mW.

Index Terms—DAC with level reduction, delta sigma ADC, extended dynamic range, truncation noise cancellation.

I. INTRODUCTION

VERY high resolution, ultra-low distortion and relatively low power ADCs are needed in many instrumentation and audio applications. This goal can be achieved by high order sigma delta modulators with relatively high oversampling ratios (OSR)[1]. However, when power is a concern, it is necessary to find the best trade-off among order, oversampling ratio and number of quantization bit. Using a relatively large number of bits in second order modulators permits designers to achieve 100+ dB SNR. However, with the increased number of bits in feedback DACs, the unity elements in the DACs are scaled to a smaller size, and more sensitive to other mismatch sources (like cross-coupled capacitance), which may become dominant compared to the random mismatch between the unity elements and need more effective DEM to shape the extra errors. Therefore, the indispensable dynamic element matching (DEM) for transforming elements mismatch into a shaped noise becomes problematic for more than 3 bits [2], [3].

Another critical point is the capability to minimize the modulator's distortion for all the amplitudes in the dynamic range. When a small signal is applied to a second order SDM, the problem of idle tones often causes performance degradation. Dithering is a common method of alleviating this issue but needs

extra hardware to implement [4]. At large signal levels, the distortion terms can dominate the SNDR because of the saturation in the sigma delta loop. Power dissipation may be increased to reduce the severity of this problem by enlarging the reference voltage of the SDM. But it causes the higher quantization noise, which may increase the in-band noise floor.

This paper proposes several techniques to achieve a very high SNR and low THD with a second order scheme and 5-bit quantization. Some of them were published in [5]. But in this paper, these techniques will be further improved to achieve a much lower THD with input amplitude closer to full scale. In order to obtain an effective DEM, the numbers of bits in the DACs are reduced to 2 and 3.5-bit by the use of a signal processing block in the feedback loop shown in Fig. 1. The 5-bit quantization grants a sufficient SNR performance at $\text{OSR} = 128$. But the final digital output is truncated to 3 bits by using the signal processing block with high-order shaping for the injected error. The shaped truncation error also performs as dithering in the loop without increasing the in-band noise floor, alleviating idle tone problem when small signal levels are applied. With the signal processing block, the truncation and saturation errors are compensated and cancelled, extending the dynamic range for a maximum input signal swing up to full scale. Furthermore, the whole implementation has a strong tolerance to analog imperfections. With the 8 MHz sampling frequency, it is possible to limit power dissipation for the entire modulator to 14.7 mW.

The basic architecture of the SDM is shown in Fig. 1. It is a conventional second order scheme [6], [7] with a feed-forward path for reducing the voltage swing at the output of the first integrator. The gain by 2 of the second integrator was moved to the digital domain to halve the swing of the second integrator. The main purpose is to reserve the sufficient swing range of the second integrator for the carried truncation errors from the first integrator to compensate when the input signal is close to full scale. The final output of the modulator obtained by the signal processing block is 3-bit at the clock frequency.

The paper, after defining design goals in Section II, describes in Section III the signal processing technique used to reduce the number of bits in the DACs and digital output. Section IV illustrates the behavioral simulations and Section V describes the circuit implementation. Section VI presents the experimental results, before the conclusions.

II. DESIGN GOALS AND MOTIVATIONS

This design aims at obtaining three key features: a high number of levels in the quantizer, small numbers of levels in the DACs and a high SNDR until full-scale input.

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Fig. 1. Block diagram of the proposed sigma delta modulator with reduced levels for internal DACs and signal processing

Increasing the levels in a quantizer does not cost much in terms of power consumption. One more bit of resolution requires to increase the OSR by 1.31 for a second order modulator and 1.22 for a third order one. Since the bandwidth is proportional to the square of current, the power consumption of op-amps increases by 71% and 48%, respectively. Such an increase of power dissipation is normally more than what is required to double the number of comparators in the flash ADC, until relatively high resolutions (roughly 5–6-bit). But increasing the numbers of levels in the DACs makes layout complexity grow exponentially and is more sensitive to other mismatch sources.

The above motivates the second goal, namely using small numbers of levels in the DACs to ease the DEM implementation and practical layout design. Yu *et al.* [8] demonstrated reduced levels in the DACs with smaller quantization noise power, but the injected extra large truncation noise offsets the benefit, even saturating the sigma delta loop at an earlier stage. Therefore, its peak SNDR was obtained far before the input signal reached full scale. Therefore, how to avoid early saturation that limits the THD is the third goal of this design. In addition to saturation, THD can also be caused by analog imperfections and special care on these limits is an important part of design goals.

III. BIT REDUCTION AND CARRY-OVER TECHNIQUES

As shown in Fig. 1, the signal processing block receives the 5-bit quantizer output and generates 3-bit output (D_{out}). Moreover, it generates low-resolution controls of primary and secondary internal DACs. The reduction of the output bits is beneficial for the successive decimation filter. It is used because a one-step reduction from 5-bit to the 2-bit of primary DAC control is problematic. Fig. 2 shows the performed operation for truncation. The 5-bit input is divided into 3-bit MSB ($\text{OUT} + \varepsilon$) and 2-bit LSB ($-\varepsilon$). The 3-bit part is the output signal while the 2-bit truncation error is fed back and added to OUT after a $4T_s$ delay (T_s is the clock period). Therefore, D_{out} in Fig. 1 is affected by two errors, the quantization error and the truncation error passed through a $(1 - z^{-4})$ filter. If the two errors can be assumed equivalent to white noise, the effect of the second order

Fig. 2. Block diagram of the truncation and bit splitter.

modulator shapes both with a second order NTF. Since the truncation is from 5-bit to 3-bit, the amplitude of truncation error is assumed 4 times of the quantization. Therefore, the transfer function is approximated to

$$D_{\text{out}} \approx IN + 2(1 - z^{-1})^2 \varepsilon_Q + 2(1 - z^{-1})^3 (1 + z^{-1})(1 + z^{-2}) \varepsilon_T \quad (1)$$

summation of saturation and truncation error, the input of “Sat” block in Fig. 2 can accommodate a signal even larger than 0 dB_{FS}. As shown in Fig. 1, the error ε_1 is fed to two paths. One is fed back to the 1st integrator with D_{out} , the other is carried over in digital domain by the transfer function (H_{1D}) that mimics the corresponding analog path (H_{1A}), and its effect is subtracted at the input of the second integrator and cancelled. Hence, it does not exist in the SDM final output as shown in (1). Because of the carried error of ε_1 , the input of the secondary DAC is larger than full scale. The block named “truncation & bit splitter 2” shown in Fig. 1 limits the signal amplitude to $\pm 1.5V_{ref}$ that corresponds to a 3.5-bit DAC instead of 3-bit one. A new added error ε_2 is carried over all the way to the flash ADC and finally cancelled at the output of the ADC. DAC2 uses more unity capacitance to ensure a $\pm 1.5V_{ref}$ range. The choice of extending the range of DAC2 to $\pm 1.5V_{ref}$ results from a trade-off that accepts an increased second integrator swing for a more favorable feedback factor.

The signal processing of Fig. 1 can be implemented easily and accurately; however, because of analog imperfections, H_{1D} is not an exact replica of the analog counterpart (H_{1A}), causing leakage of the truncation error. Since the goal is to achieve a high-resolution ADC design, the architecture needs to alleviate the limits of analog imperfections. The processing blocks which contribute the truncation errors also shape the spectrum of these errors. The equations of the integrators with analog imperfections are shown as follows:

$$\begin{aligned} H_{1A}(z) &= H_{1D}(z)(1 + \delta_1(z)) \\ H_{2A}(z) &= H_{2D}(z)(1 + \delta_2(z)) \end{aligned} \quad (4)$$

which assume $\delta_1(z) \ll 1$ and $\delta_2(z) \ll 1$. Therefore, the transfer function in Fig. 1 can be written as

$$\begin{aligned} D_{out} &\approx IN + 2(1 - z^{-1})^2 \\ &\cdot \left[\frac{-0.5z^{-2}}{(1 - z^{-1})^2} \delta_1(z)\varepsilon_1 + \frac{-z^{-1}}{1 - z^{-1}} \delta_2(z)\varepsilon_2 + \varepsilon_Q + (1 - z^{-1})^4 \varepsilon_T \right] \\ &= IN + 2(1 - z^{-1})^2 \left[c_1(z)\varepsilon_1 + c_2(z)\varepsilon_2 + \varepsilon_Q + (1 - z^{-1})^4 \varepsilon_T \right]. \end{aligned} \quad (5)$$

To make $c_1(z)\varepsilon_1(z)$ and $c_2(z)\varepsilon_2(z)$ much smaller than $\varepsilon_Q\delta_1(z)$ and $\delta_2(z)$ are required to be sufficiently small. If $\varepsilon_1(z)$ and $\varepsilon_2(z)$ are not shaped, to minimize the noise leakage in their cancellation process, the analog components should be extremely well matched and the opamps should be designed with very large DC gain and high speed. This makes the whole design extremely sensitive to the analog imperfection.

In order to resolve the problem mentioned above, ε_1 and ε_2 are shaped through $H(z)$ as listed in Fig. 2

$$\begin{aligned} \varepsilon_1 &= (1 - z^{-1})^2 \varepsilon_{T1} \\ \varepsilon_2 &= (1 - z^{-1}) \varepsilon_{T2} \end{aligned} \quad (6)$$

in which ε_{T1} and ε_{T2} , assumed with white spectrum, are the truncation errors injected into DAC1 and DAC2. With noise

Fig. 3. Power spectral density for truncation and quantization errors of the proposed sigma delta modulator.

shaping shown in (6), the following conditions are much easier to be met within the signal bandwidth

$$\begin{aligned} |\delta_1(z)\varepsilon_{T1}| &\ll |\varepsilon_Q| \\ |\delta_2(z)\varepsilon_{T2}| &\ll |\varepsilon_Q| \end{aligned} \quad (7)$$

which represent that in (5), the quantization noise dominates the in-band noise floor. The immunity of analog imperfections is dramatically improved when in-band noise of ε_1 and ε_2 are greatly attenuated by noise shaping. In the next section, a behavioral model is implemented in order to specify the circuit requirements

IV. BEHAVIORAL SIMULATIONS

The architecture has been extensively simulated at the behavioral level to estimate specifications of op-amps and kT/C limit. The study was done using the behavioral model described in [9] that accounts for finite gain, bandwidth and slew-rate of op-amps and thermal switched noise. The use of high-performance op-amps and large matched capacitances gives the diagram of Fig. 3. It shows the total noise power spectrum and its integral. High frequency spectrum is dominated by truncation noise. It can be observed that the slope has the 3rd-order noise shaping with 1 zero at f_N and 2 complex conjugate zeros at $f_N/2$, as predicted. The in-band noise is the one with a second-order shaping. The accumulated in-band noise determines the SNR is also plotted. Result gives 118 dB with almost full-scale input.

Performance worsens when the analog limitations are accounted for. Fig. 4 shows the behavioral simulation results with finite amplifier gains and integrator gain mismatch. Thermal noise (kT/C) is also considered. Based on simulation results, the modulator works properly with 60 dB amplifier open-loop DC gain and 1% gain mismatch between input and feedback capacitors without significant degradation of the SNDR. Therefore, gain boosted amplifiers or multi-stage amplifiers are not necessary because a simple single-stage scheme is enough to achieve 60 dB DC gain. Moreover, the 1% mismatch is certainly ensured by currently available process technologies. The kT/C limit defines the needed capacitance, about 6 pF. The demanded GBW and slew-rate are 75 MHz, 100 V/ μ s and

Fig. 4. SNDR comparison with different amplifier open-loop gains and integrator gain errors caused by capacitor mismatch.

Fig. 5. SQNDR of second-order 5-bit SDM with 5-bit feedback DACs.

50 MHz, $50 \text{ V}/\mu\text{s}$ for the first and second op-amp respectively. Figures (in Fig. 4) obtained from behavioral simulations are the specifications of the basic blocks used for the implementation.

Another important feature is obtaining peak of SNR with close to full-scale input. This feature is obtained by this architecture that clips the control of the first DAC but carries the error over and compensates for it as an extra input driving the next

DAC. The possible effect of the saturation of the second DAC is almost imperceptible because its range is extended. Fig. 5 shows that this second-order 5-bit SDM with oversampling rate 128 grants the in-band signal-to-quantization-noise-and-distortion ratio (SQNDR) that grows steadily until $-0.6 \text{ dB}_{\text{FS}}$. With the carry-over technique, the peak of SQNDR is extended to $-0.16 \text{ dB}_{\text{FS}}$.

Fig. 6. Simplified circuit diagram of the first integrator with current-type output choppers.

V. CIRCUIT IMPLEMENTATION

The offset and flicker noise of the op-amp in the first stage are filtered out with a chopper stabilized source-cross-coupled operational transconductance amplifier (OTA). It is a class-AB single-stage topology [10] with current output chopping as shown in Fig. 6. Compared to a class-A amplifier, this amplifier obtains a high slew rate, good settling behavior and better power efficiency. The output chopper uses a current chopping instead of a voltage chopping in order to achieve fast settling. Voltage-type choppers usually have small capacitors across the feedback of the amplifiers to maintain unbroken feedback loops when the choppers are switching [11], introducing an integrator gain error. The small feedback capacitors are not needed in current-type choppers. But complete turn-off in switching causes ripples and slows settling in current-type choppers. This problem can be resolved with the chopper clocks overlapped on rising and falling edges [12]. Bootstrapped input switches are applied in the first integrator to avoid the distortion dominated by the nonlinearity of on-resistance. The second OTA is a folded-cascode class-A amplifier capable to meet the reduced specifications as required for the second stage integrator.

The scheme of 5-bit flash ADC uses current-mode interpolated topology [13] with six voltage to current converters (V-I) and five current interpolators. The solution reduces loading on the previous stage and obtains low power consumption. Fig. 7 shows the block diagram of the 5-bit quantizer. The V-I is a differential pair with linearization granted by source degeneration. Interpolation of produced current uses a current ratio technique to obtain six intermediate currents transformed into voltages and compared with the reference voltages generated by the resistor ladder. This quantizer has a DNL better than ± 0.5 LSB when tested as a separate part.

VI. EXPERIMENTAL RESULTS

The die photograph (Fig. 8) shows also the floor plan of the design. The die was packaged in a 48-pin leadless lead-frame

Fig. 7. Block diagram of 5-bit current-mode flash ADC.

Fig. 8. Die photograph of the 5-bit delta sigma modulator with reduced number of levels for the internal feedback DACs.

package (LLP) and extensively AC and DC tested. The test setup uses a FPGA board for data collection and decimation filtering made with multi-stage comb filters combined with a final gain stage filter to compensate for gain droop. The implementation yields that the pass-band which is less than 0.005 dB ripple is up to 0.45 times of output data rate (ODR), the -3 dB frequency is at $0.49 \cdot \text{ODR}$, and stop-band with attenuation larger than 105 dB is after $0.55 \cdot \text{ODR}$. The latency of the digital filter is

Fig. 9. Screen capture of real-time 2M-point FFT before the decimation filter.

Fig. 10. Screen capture of real-time 128K-point FFT after the decimation filter.

less than $72/\text{ODR}$. For 8 MHz clock rate and 128 downsampling rate, ODR is 62.5 KSPS. It turns into 0.005 dB ripple pass-band is at 28.125 KHz and -3 dB pass-band is at 30.625 KHz. The board provides a real-time FFT output. The supply voltage for the analog circuit is 3.3 V and for the digital circuit is 1.8 V. A 3.3 V off-chip reference is used in the experiments as V_{ref} . An external low jitter crystal oscillator provides 8-MHz clock. The 1-KHz input signal was produced by an Audio Precision signal generator with ultra low THD. Fig. 9 shows screen capture of the real-time 2M-point FFT with Blackman-Harris window obtained from the modulator's outputs. A SNDR of 105.76 dB and a THD of -120.48 dB (which was less than 1 ppm when the sinusoidal input was close to the modulator's full scale) were achieved at $2.283 V_{\text{RMS}}$ (root-mean-square) input power. Noises were integrated from 20 Hz to 31.25 KHz, which was the Nyquist bandwidth after downsampling a factor by 128. The performance was obtained by averaging the results over 100 measurements. Fig. 10 shows the output spectrum with real-time 128 K-point FFT after the decimation filter.

Fig. 11. Measured SNDR versus different input amplitudes.

Fig. 12. Measured SNDR versus frequencies after the decimation filter.

Fig. 11 indicates the SNDR versus input signal swing normalized to full scale after the decimation filter. The peak SNDR was measured at $-0.18 \text{ dB}_{\text{FS}}$ with 1-KHz sine tone. The modulator saturates at around $-0.12 \text{ dB}_{\text{FS}}$. With zero input signals, the in-band noise was $9.8\text{-}\mu\text{V}_{\text{RMS}}$, giving a 107.4 dB DR. The power consumption for the core (integrator 1, integrator 2, flash ADC and DSP for level reduction and truncation filters) totaled about 14.7 mW (12.3 mW for the analog core and 2.4 mW for the digital core) giving a 1.44-pJ/step figure of merit (FoM). Table I summarizes the comparison of the previous state-of-art works with around 16-bit ENOB. Fig. 12 shows the SNDR versus frequencies of the sine inputs at the fixed $-0.18 \text{ dB}_{\text{FS}}$ amplitude after the decimation filter. Noise and distortion were integrated from 10 Hz to 31.25 KHz. The SNDR varies from 102.5 dB, caused by the attenuation of the decimation filter at the signal band edge to 105.9 dB in the signal frequency band.

VII. CONCLUSION

This architecture of the SDM reduced the number of levels in the internal DACs and enhanced the tolerance to analog imperfections to obtain high performances with low power dissipation. The extended dynamic range allowed up to $-0.12 \text{ dB}_{\text{FS}}$ input signal swing. The measured results for peak

TABLE I
COMPARISON OF THE PREVIOUS STATE-OF-THE-ART WORKS WITH AROUND 16-BIT ENOB

	BW (Hz)	DR (dB)	Peak SNDR (dB)	Power (mW) (analog)	Process (CMOS)
[1]	20K	106	99	18	0.35 μ m
[14]	20K	102	95	37.3	0.18 μ m
[15]	20K	114	106	55	0.35 μ m
This work	31.25K	107.4	105.9	14.7 (with DSP)	0.18 μ m

SNDR at -0.18 dB_{FS} showed that this modulator had a more than 17.4-bit DR and a better than 17.2-bit ENOB.

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