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A high efficiency 4-output single inductor DC–DC buck converter with self boosted snubber

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Abstract This paper presents a single-inductor 4-outputs DC–DC buck converter. In order to independently regulate the four output voltages, a multiple control loop operates on linear combinations of the output voltage errors. An original self-boosted snubber circuit enables load power switches control signals boosting without area and power efficiency penalties. The circuit, fabricated using a 0.5-μm CMOS process, provides four output voltages that can be independently regulated from 0 V to the used supply voltage −500 mV. The supply voltage can range from 2.3 up to 5 V. The overall minimum and maximum output currents are 0.15 and 1.8 A, respectively. The measured maximum cross regulation is 40 mV/V with a peak of power efficiency equal to 85%.

Keywords DC–DC converters · Buck converter · Single-inductor multiple-output

1 Introduction

Many battery-operated systems such as digital cameras, personal digital assistants, cellular phones, MP3 players, medical diagnosis systems, etc. use, or are going to use, multi-processor architectures with multiple and dynamically regulated supply voltages. The common goal is to maximize the battery life by using the optimal supply voltage in each block. The major limit to the trend is the need of many DC–DC voltage regulators [1] with a bulky and expensive inductor for each of them. A possible solution is to increase the switching frequency of the DC–DC converter for reducing the value of inductors, [2]. Another method is to use DC–DC converters capable to generate many outputs with a single inductor (Single Inductor Multiple Output, SIMO), [3–8]. The first approach, that increases the dynamic losses, enables a reduction of the PCB area but keeps the number of external components unchanged. The SIMO costs extra switches, but improves the overall reliability and diminishes the PCB area.

In single-inductor multiple output (SIMO) DC–DC converters design, it is necessary to time-share the inductor current between various loads. For this, the feedback loop that regulates the voltage becomes a multi-feedback loop with eventual stability problems and possible ringing of the outputs. In addition, for buck architectures that regulate a high input voltage into a lower one [9, 10], it is necessary to use extra power switches on the load side, [3, 7, 8]. For these kinds of converters, the switches must separate voltages that can have a significantly different value. Therefore, the power switch drivers must account for problems that are specific of the multiple output function and an adequate driving strategy, able to ensure adequately low on-resistance and, hence, high power efficiency performance, has to be studied.

In this paper we present a single-inductor DC–DC buck converter with four independently regulated outputs, fabricated in a 0.5-μm CMOS process. The adopted multiple control loop architecture and power load switches strategy allow independent regulation of the four outputs from 0 to 500-mV below the used supply voltage. The buck converter can operate with input voltages in the range 2.3–5 V.

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The overall driving capability is 1.8 A, with a single-channel maximum output current of 0.8 A. The original self-boosted snubber circuit used to obtain load power switches high voltage control signals requires a minimum overall converter output current of 150 mA. The measured peak of power efficiency is 85%.

Section 2 describes the chip architecture, discusses the adopted multi-control loop implementation, the inductor time sharing and the load power switch strategy. Then, Sect. 3 presents circuit implementation details, while Sect. 4 provides the collected experimental results.

2 Chip architecture and design considerations

The operation of a conventional single-inductor, single-output DC–DC buck converter with PWM voltage mode control is well known, [1]. The output voltage is subtracted from the input setting voltage to obtain the output voltage error, ε, which is amplified and compared with a saw-tooth signal with period $T = 1/f_s$, f_s being the converter switching frequency. The resulting pulse drives the DC–DC power switches.

When designing a buck converter with multiple output branches, it is necessary to use multiple control loops, which ensure the proper single inductor current time sharing among different loads. Figure 1 shows the proposed single-inductor 4-output buck converter block diagram. The high-side and low-side power switches, MP and MN, implement the conventional buck structure, while the four n-channel MOS switches (namely, SW_1, SW_2, SW_3, and SW_4) share the inductor current to sustain the four output voltages, V_{oi} (i = 1, 2, 3, and 4).

In multiple-output DC–DC converters, an important design issue is the power switch driving strategy, which affects the overall system performance, in terms both of area and power consumption. In any single or multiple output DC–DC converter, the switch connected to the battery and the switch connected to ground are obviously

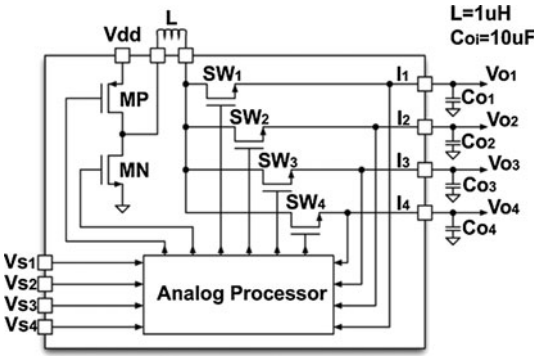

Fig. 1 Single-Inductor 4-Output buck converter block diagram

made by p-channel and n-channel devices, respectively. By contrast, the switches on the load side can be implemented with a p-channel, an n-channel or a complementary switch. The choice depends on the expected regulated voltage and on the cost-efficiency trade-off. If the regulated voltage is relatively large, much higher than the transistor threshold voltage, then the use of a p-channel device is a good solution: the overdrive voltage is sufficiently large and the series conductance caused by the extra switch can become affordable with a reasonable transistor aspect ratio. However, as well known, the threshold voltage changes because of the body effect and, in order to cancel it, it is necessary to connect the bulk to the source. This is allowed with a single output and n-well technologies, but it is not straightforward with multiple outputs because of the possibility of having the terminal connected to the inductor at a voltage that is the higher than the considered output. This limit is not negligible because the body effect can worsen the threshold voltage by 100–200 mV, thus increasing the series resistance significantly. The solution to this problem is to connect the n-well to the highest voltage among the switched terminals, [11]. Another possible solution is to use complementary power switches, but there are limits: the silicon area is almost doubled and the power required to charge and discharge the gate of the power transistors is significantly increased. Therefore, complementary switches can be used only for applications with very low current, for which the sizing of the power switches is not an issue. The other possible solution is to use an n-channel transistor, which for being properly closed requires a voltage higher than the power supply. As known, this can be achieved using charge pumps, [12]. The switching of one or more pumping capacitances enables reaching as high voltages as required, for example, in non-volatile memories. However, in the case of multiple output boost schemes, the gate capacitance of the power transistor can be as high as 15 pF and the corresponding charge that must be provided leads to area and efficiency issues. In this paper, a different approach, named self boosted snubber, ensures to overcome the above limits. The operation of the self boosted snubber circuit will be described in the next Section of this paper. However, the use of the proposed solution allows using n-channel devices (with grounded bulk), as shown in Fig. 1, without power efficiency penalties and saving silicon area.

The buck converter of Fig. 1 operates in continuous mode, but the current delivered to the output capacitors, C_{oi}, is discontinuous because it goes to zero when the corresponding switch opens. This and the inductor current time sharing can be appreciated in Fig. 2. When the high-side switch MP is on, the inductor stores energy from the power supply and delivers energy to the loads. Therefore, during this time the inductor current rises with positive

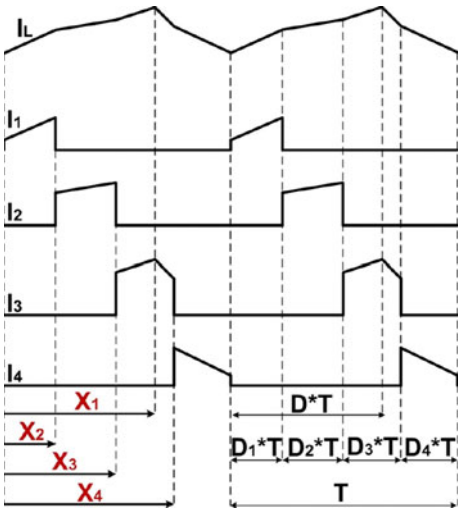

Fig. 2 Single-Inductor 4-Output buck converter inductor current time sharing

slope. When the low-side switch MN is on, the inductor delivers energy to the loads and during this time the inductor current falls with negative slope. In the proposed 4-output DC–DC converter, the PWM control has to determine the buck switching main duty-cycle and four inductor current time sharing slots. The regulator will, hence, process four control equations and the system will manage four control loops with the four output voltage errors as input. A main duty cycle D and four sharing duty cycles D_i can be defined. They can be expressed as

$$D = \frac{T_{on,MP}}{T} \tag{1}$$

$$D_i = \frac{T_{on,SW_i}}{T} \tag{2}$$

respectively. In order to identify a set of control equations, the problem is to find a vector $\mathbf{X}$ of four time instants as a function of the input $\boldsymbol{\varepsilon}$

$$\mathbf{X} = f(\boldsymbol{\varepsilon}) \tag{3}$$

The used solution foresees a linear processing of $\boldsymbol{\varepsilon}$, leading to a linear system of equations

$$\begin{cases} X_1 = a_{11}\varepsilon_1 + a_{12}\varepsilon_2 + a_{13}\varepsilon_3 + a_{14}\varepsilon_4 \\ X_2 = a_{21}\varepsilon_1 + a_{22}\varepsilon_2 + a_{23}\varepsilon_3 + a_{24}\varepsilon_4 \\ X_3 = a_{31}\varepsilon_1 + a_{32}\varepsilon_2 + a_{33}\varepsilon_3 + a_{34}\varepsilon_4 \\ X_4 = a_{41}\varepsilon_1 + a_{42}\varepsilon_2 + a_{43}\varepsilon_3 + a_{44}\varepsilon_4 \end{cases} \tag{4}$$

It is evident that it is convenient to use, as vector of the input variables, the errors $\varepsilon_i = (V_{oi} - V_{si})$. Therefore, we obtain

$$\mathbf{X} = \mathbf{T}\boldsymbol{\varepsilon} \tag{5}$$

The use of different $\mathbf{T}$ matrixes leads to different control strategies. As an example, a diagonal matrix $\mathbf{T}$ with all diagonal coefficients equal to one means using a single error for the control of each of the times. Although this can be acceptable for a single-inductor dual-output converter, [11], it is problematic with four loops because instability might occur in many regions of operation. The matrix $\mathbf{T}$ used for this design is given by

$$\mathbf{T} = \begin{bmatrix} +1 & +1 & +1 & +1 \\ +1 & -1 & -1 & -1 \\ +1 & +1 & -1 & -1 \\ +1 & +1 & +1 & -1 \end{bmatrix} \tag{6}$$

The chosen matrix represents the best trade-off between complexity and effectiveness. Using the matrix given in (6), the set of control equations used can be expressed as

$$\begin{cases} X_1 = \varepsilon_1 + \varepsilon_2 + \varepsilon_3 + \varepsilon_4 \\ X_2 = \varepsilon_1 - \varepsilon_2 - \varepsilon_3 - \varepsilon_4 \\ X_3 = \varepsilon_1 + \varepsilon_2 - \varepsilon_3 - \varepsilon_4 \\ X_4 = \varepsilon_1 + \varepsilon_2 + \varepsilon_3 - \varepsilon_4 \end{cases} \tag{7}$$

In order to ensure the stability to the system, it is necessary to associate the control voltages X_i to proper control variables. In the considered case X_1, X_2, X_3, and X_4 are related to the duty-cycles D, D_1, $D_1 + D_2$, $D_1 + D_2 + D_3$, respectively. In particular, for positive X_i the corresponding duty-cycle is increased with respect to the nominal value, while for negative X_i it is decreased.

Figure 3 shows the conceptual scheme of the 4-output control system together with the PWMs output pulses. The transfer function H(s) in the main path is a first-order zero-pole filter that achieves the loop compensation, while blocks A in the sharing paths are just amplifiers. The main path, driven by $Y_1 = H(s)\ X_1$, controls the main switches MP and MN, while the other paths, driven by $Y_2 = AX_2$, $Y_3 = AX_3$, and $Y_4 = AX_4$, manage the sharing of the inductor current, thus determining the four time-sharing slots, as depicted in the system block diagram of Fig. 4.

3 Circuit description

In order to minimize the number of active stages and, hence, the system quiescent power consumption, the analog processor of Fig. 3 has been realized by using a switched capacitor discrete time circuit. This choice enables the implementation of inverting and non-inverting blocks. Figure 5 shows the scheme for the main processing path. It consists of three blocks. The first section combines the errors and provides a gain; the second is the first order zero-pole switched-capacitor filter. Capacitor C_5 and voltage V_b are used to achieve a DC level shift. The third block is a the flip around double sample-and-hold, necessary to decouple the filter from the PWM, thus limiting the kick-back from the switching part and eliminating the glitches produced by the switching from phase 1 to phase 2. The

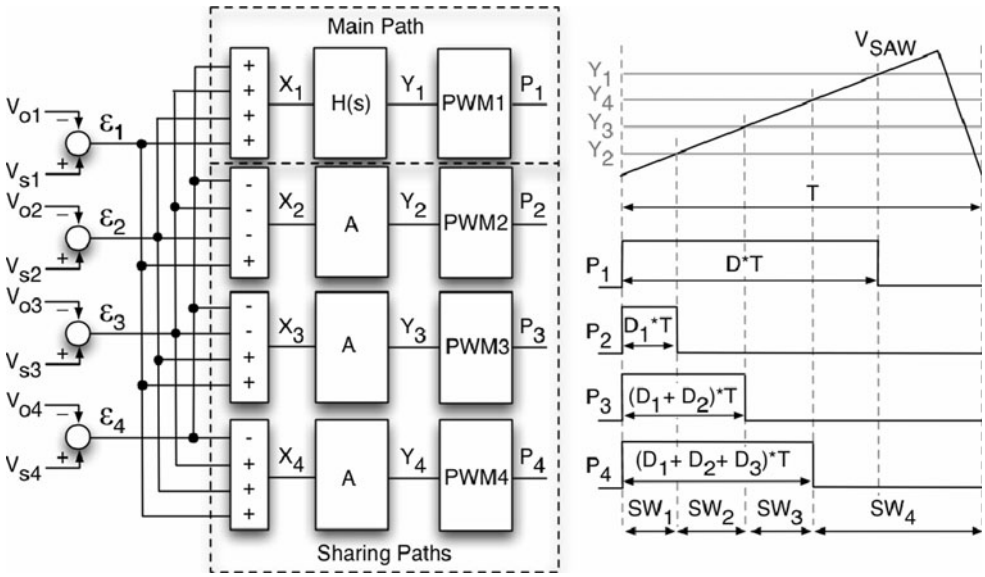

Fig. 3 Conceptual scheme of the analog processor and PWMs output pulses

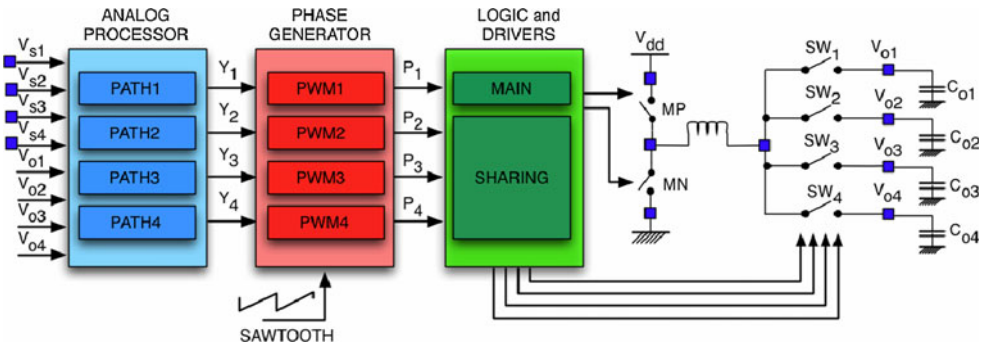

Fig. 4 Single-inductor 4-output system block diagram

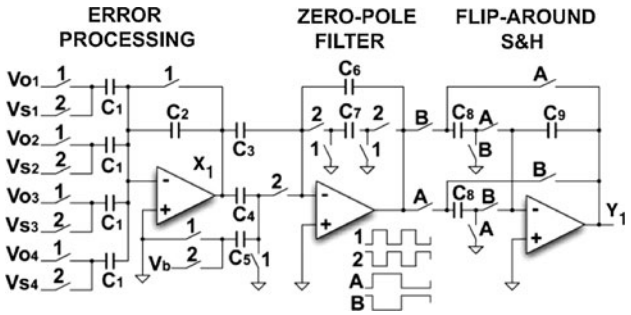

Fig. 5 Analog processor main path switched capacitor implementation

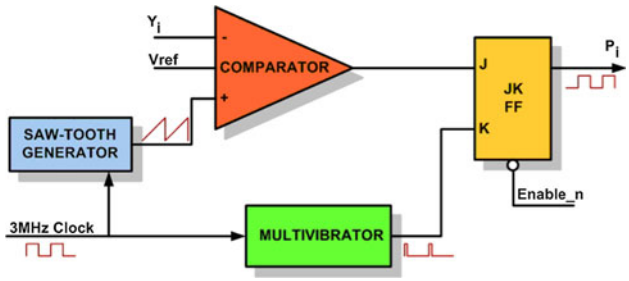

Fig. 6 PWM modulator block diagram

other processing channels (referred to as Sharing Paths in Fig. 3) do not require filtering and are realized with only two sections. One is to process the errors, providing gain and shifting the DC level, while the other is the sample-and-hold. The unity capacitance used in the SC circuit is 100 fF. The operational amplifiers (OTAs) are based on a conventional two-stage architecture with pole-splitting compensation. The two-stage topology has been preferred to ensure the maximum output voltage swing.

The conventional scheme of Fig. 6 realizes the four PWM modulators. They consist of a voltage comparator, a saw-tooth generator, a monostable multivibrator, and an enabled JK flip-flop. At the beginning of each clock period, the multivibrator output signal forces the circuit output to zero. The modulator output voltage rises to the high level when the input voltage crosses the saw-tooth waveform. The continuous time voltage comparator is realized with a n-channel differential gain stage with resistive loads. A common-mode feedback ensures the proper output voltage level. Reference voltage V_{ref} sets the nominal value of the duty-cycle.

As mentioned in the previous Section, the four load side power switches (SW_1, SW_2, SW_3, and SW_4 in Fig. 1) need proper boosting when turning on. Self boosted drivers (Fig. 7) solve the problem. Since all the paths to ground are open when the switches are all off (during the non-overlap period), the inductor current flows trough diode D and charges the internal capacitor $C_{int} = 170$ pF, which is connected in parallel with an external capacitor $C_{ext} = 430$ pF, to boost the voltage. At the end of the non-overlap period the i-th control signal coming from the analog processor goes low, which turns MN_i off and switches MP_i on. Capacitors C_{int} and C_{ext} share their charge with the gate of the power switch SW_i, which turns on when its gate-source voltage reaches the threshold voltage. At this time, the voltage at the right terminal of the inductor drops down and diode D turns off. The ESD clamp included in the pad required to connect C_{ext} limits the boosted voltage to about 5 V, thus granting safe operation of the circuit. To ensure proper control of MN_i through MP_i, the logic signal provided by the analog processor is almost doubled by means of a charge pump (CP), [13, 14]. The sharing logic provides the four load switching driving phases from the PWM digital outputs. To avoid short circuits among different outputs during the sharing commutations, a digital feedback has been added. The feedback path senses the load switches gate voltages and provides a time-disoverlap between the driving phases. Inverter chains in the feedback path obtain the required disoverlap.

4 Measurement results

The proposed single-inductor 4-output DC–DC converter has been fabricated using a 0.5-μm, two poly, five metal levels CMOS technology. Figure 8 shows the chip microphotograph. The total area is 3.5 mm × 3.8 mm with 1.2 mm^2 used for analog processing. Table 1 summarizes the used device sizes. The converter switching frequency is 3 MHz. It is worth to point out that an improved measurement set-up and an optimized PCB allowed us to obtain better performance with respect to what published in [3]. Experimental results show that, with a 2.3-V minimum supply, it is possible to independently regulate the four outputs in the range 0–1.8 V with a total current capability of 1.2 A. With a higher supply voltage, the 1.8 A overall driving capability provides the maximum single-channel current of 0.8 A in one channel and the remaining in the others. Lower currents are obviously possible, but the minimum average inductor current needed by the self-boosting switch drivers is 0.15 A. The voltage ripple is lower than 90 mV under any operating conditions. The circuit operates with supply voltages up to 5 V. However, since the ESD protection on the self-boosted drivers output limits the boosted voltage to about 5 V, the regulated outputs can only go up to 3.6 V. For all measurements hereinafter the used power supply voltage is 2.3 V.

Figure 9 shows three of the four output voltages ($V_{out2} = 1$ V, $V_{out3} = 1.2$ V, $V_{out4} = 1.4$ V) and the switching node voltage waveforms in the steady state. The output currents are 200, 240, and 300 mA, respectively. In

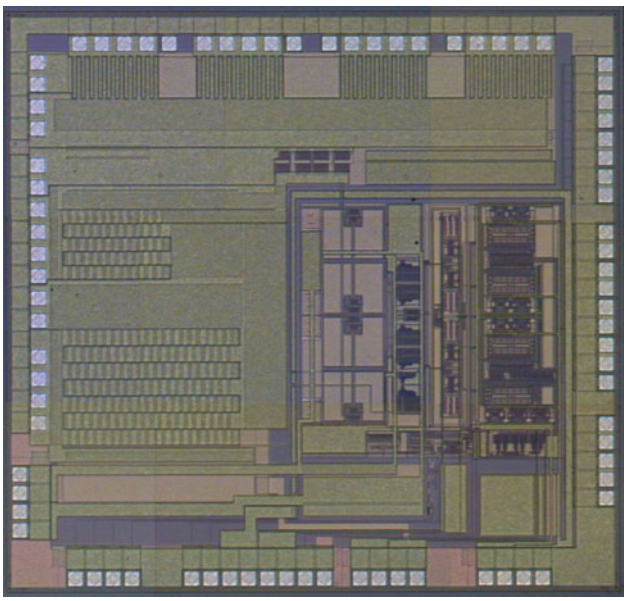

Fig. 8 Chip microphotograph

Table 1 Used devices sizes (i = 1, 2, 3, and 4)

Device	Size	Unit of measurement
L (external)	1	μH
C_{oi} (external)	10	μF
MP	300/0.5	mm/μm
MN	60/0.5	mm/μm
SW_i	30/0.5	mm/μm

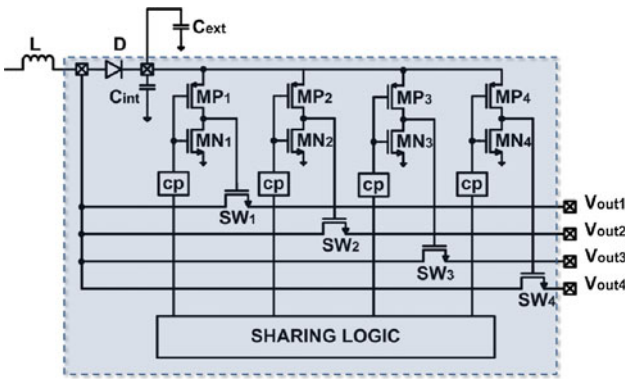

Fig. 7 Self-boosted snubber circuit

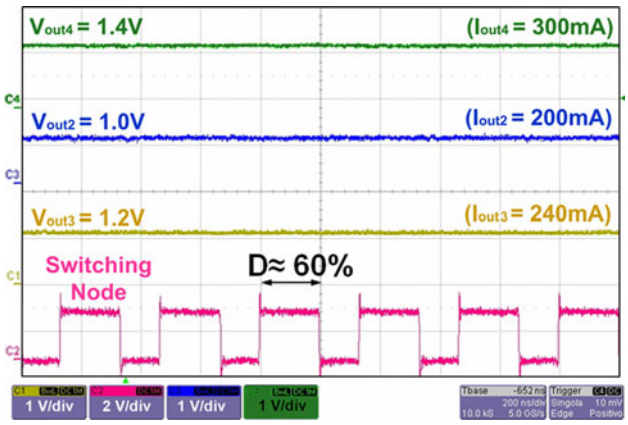

Fig. 9 Measured output and switching node voltages

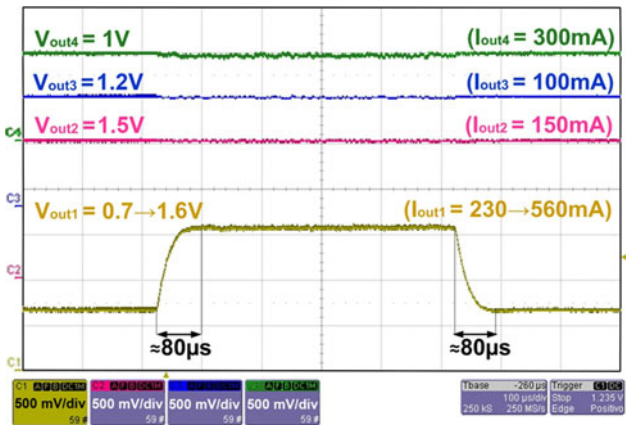

Fig. 11 Cross-regulation measurement

this measurement, $V_{out1} = 1.6$ V, and $I_{out1} = 350$ mA. The stability of the main control loop is demonstrated by the periodical switching node voltage waveform. The main duty in this case is about 60%.

Figure 10 shows an output voltage ripple measurement. The four output voltage waveforms in steady state are AC coupled, with a vertical scale of 50 mV. In this measurement, the outputs are set to 1.5, 1, 1.2, and 1.8 V, respectively, while the four output currents are 150, 200, 240, and 400 mA, respectively. The measured output ripple is about 65 mV, increased by some ringing ascribed to parasitic inductances. The ripple ringing looks periodic because it occurs in correspondence of the power switch commutations.

For cross-regulation measurements, an input filter slows down the transient response of the converter in order to avoid transient cross-regulation drops of the output voltages. However, the converter settles in about 80 µs, as shown in Fig. 11. In this measurement, V_{out2}, V_{out3} and V_{out4} are set at their proper voltage level (1.5, 1.2, and 1 V, respectively), while V_{out1} changes from 0.7 to 1.6 V and vice versa. The output currents are 150, 100, 300 and 230 → 560 mA, respectively.

Figure 12 shows again a cross-regulation measurement, but the output voltages that do not change are AC coupled with a 100-mV vertical scale. V_{out1}, V_{out2} and V_{out4} are set at their proper voltage level (1.4, 1, 1.2 V, respectively), while V_{out3} changes from 0.7 to 1.6 V and vice versa. The output currents are 300, 50, 155 and 280 → 640 mA, respectively. We achieved a cross-regulation of about 40 mV on the first and on the fourth output voltages.

In order to measure the cross-regulation transient effects, the input filter has been disabled and a step change of the second reference voltage is applied. In this measurement V_{out1}, V_{out3} and V_{out4} are set at their proper voltage level (1.4, 1, 1.2 V, respectively), while V_{out2} changes from 0.7 to 1.6 V and vice versa. The output currents are 300, 50, 155 and 280 → 640 mA, respectively. As shown in Fig. 13, the highest transient drop is of about 160 mV on the fourth output voltage, while the first output voltage drops of about 60 mV.

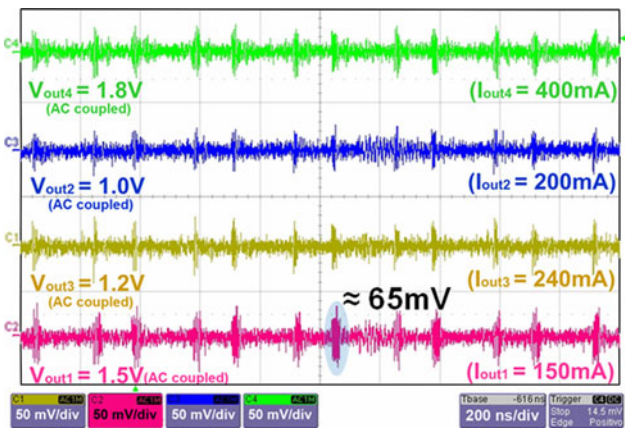

Fig. 10 Output voltage ripple measurement

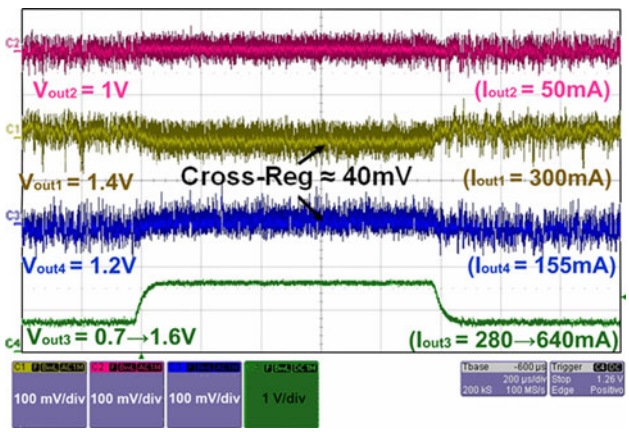

Fig. 12 Cross-regulation measurement with output voltages on channels 1, 2, and 4 are AC coupled

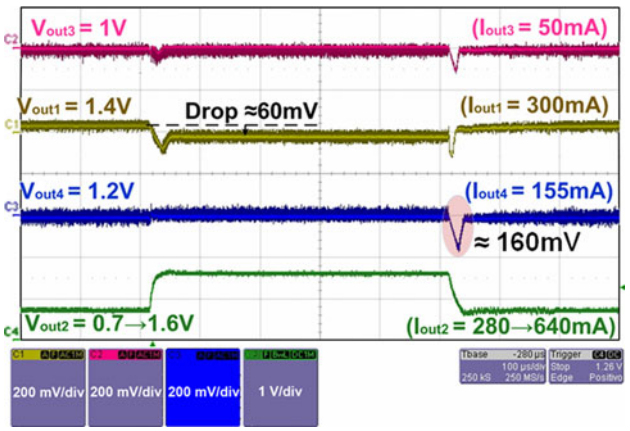

Fig. 13 Cross-regulation transient effects measurement—output channel 1, 3, and 4 are AC coupled

Figure 14 shows V_{out4}, the corresponding load switch gate voltage, the clock signal and the switching node voltage waveform. It can be noted that the self-boosted snubber circuit boost the switch gate voltage up to 5.5 V clamped by the protection pads. Some output voltage ringing of about 80 mV peak during the load switch commutations can be noted.

Figure 15 shows the measured power efficiency as a function of the fourth output current (ranging from 40 to 700 mA) with I_{out1}, I_{out2}, and I_{out3} fixed at 200, 100, and 250 mA, respectively. Using the minimum supply voltage, the measured peak of power efficiency is about 85%, a remarkable value when compared with SIMO buck converters presented in [7] and [15], which achieve a maximum power efficiency of 80.8 and 77.4%, respectively.

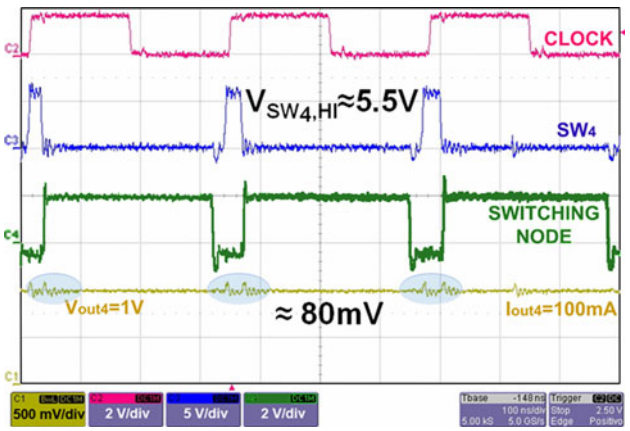

Fig. 14 Measured output voltage waveforms

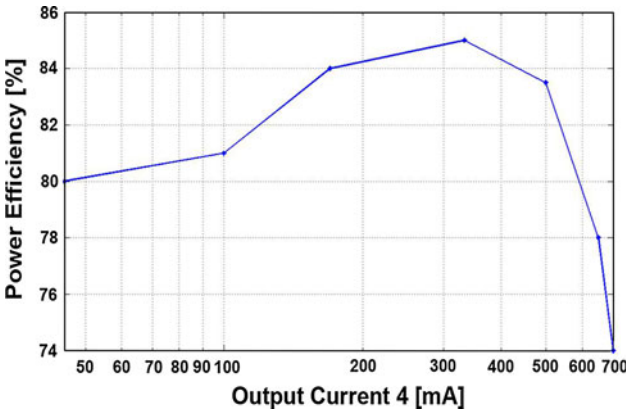

Fig. 15 Power efficiency measurement

Table 2 Performance summary

Parameter	Value
Supply voltage (V_{dd}) range	2.3–5 V
Output voltages range	0–(V_{dd}–0.5) V
Maximum output voltage	3.6 V
Total output current range	0.15–1.8 A
Single output current range	0–0.8 A
Maximum output voltage ripple	90 mV
Maximum cross-regulation	40 mV/V
Peak power efficiency (V_{dd} = 2.3 V)	85%
Process	0.5-μm CMOS
Chip area (including PADs)	3.5 mm × 3.8 mm

Table 2 summarizes the performance of the presented DC–DC buck converter. Notice that the measured maximum cross regulation is 40 mV/V.

5 Conclusion

In this paper a single-inductor buck DC–DC converter with independent regulation of four outputs is presented. Measurement results demonstrate the effectiveness of the adopted multiple control loop architecture based on a linear combination of the output voltage errors and of the original self-boosted snubber circuit. The measured peak of power efficiency is 85% and the overall driving capability of 1.8 A.

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