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Two-path double delay line based bandpass quadrature ΣΔ modulator

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A design technique for a double-delay based quadrature ΣΔ modulator is presented. The architecture uses a two-path scheme, which avoids mirror tones in the signal band and locks the intermediate frequency with the clock, thus avoiding the trimming requirement. The two-path architecture and time interleaving lead to an overall power reduction by a factor of 8.

Introduction: Quadrature ΣΔ modulators [1] are attractive solutions as they allow one to digitise the signal at low intermediate frequencies (IFs) with better spectral and power efficiency than lowpass or bandpass counterparts. This two-path quadrature architecture further improves the power efficiency by using a two-path scheme. N-path architectures use paths operating in parallel at a frequency f_S/N (f_S being the sampling frequency) and, since the power of an opamp is proportional to the square of f_S, power consumption is reduced. Topological modification and time interleaving of opamps give rise to further power reduction. The two-path approach has been used for lowpass [2] or bandpass [3] modulators but the published solutions are for normal ΣΔ schemes implemented with sampled-data integrators. By contrast, this design technique, which starts from the methodology discussed in [4], uses delay cells. This allows using flip-around schemes that relax the feedback factor of opamps, further reducing power.

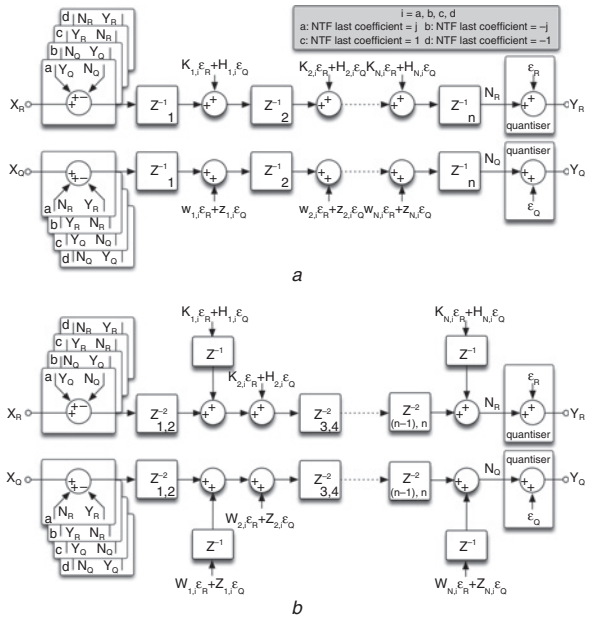

Fig. 1 *Delay based quadrature bandpass ΣΔ modulator and double delay scheme*

a Delay based quadrature bandpass ΣΔ modulator
b Double delay scheme

Method: The noise transfer function (NTF) of a quadrature ΣΔ modulator has zeros on the unit circle at the position $e^{j\phi_i}$, $i = 1, \ldots, n$. The NTF is

$$NTF = \prod_1^n \left[1 - \frac{e^{j\phi_i}}{z}\right] = 1 + \frac{a_1}{z} + ... + \frac{e^{j\sum_i^n \phi_i}}{z^n} \quad (1)$$

The last term has modulus one and phase equal to the addition of the phase of all the zeros. This method [4] limits the zero positioning to cases for which $\sum_i^n \phi_i = 0, \ \frac{\pi}{2}, \ \pi, \ \frac{3\pi}{2}$ (the last coefficient of (1) is $1, j, -1, -j$). For example, if $n = 3$, we can choose the following NTF:

$$NTF = 1 - z^{-1}(k_1 + (j)k_2) + z^{-2}(k_2 + (j)k_1) - (j)z^{-3} \quad (2)$$

where k_1 and k_2 are the design coefficients controlling the quantisation error. For IF $= f_S/12$, k_1 and k_2 are equal to 2.5 and 1.444, respectively, and give rise to a signal-to-noise ratio (SNR) higher than 55 dB with $0.125f_S$ signal band. However, choosing an odd number of zeros in the signal band is a better choice because one of the zeros is at the centre of the signal band. Moreover, an additional zero can be at the image frequency for enhancing the image rejection. The signal transfer function (STF) depends on the implementation and must be flat in the signal band.

Fig. 1*a* shows a direct implementation of (1) with the above-mentioned constraints. It is an analogue delay line with intermediate weighted injections of the quantisation noise generated in the same or the complementary processing line. The four possibilities marked with labels a, b, c, d give rise to the $\pm j$, ± 1 coefficients of z^{-n}. The weights of the intermediate noise control the position of the NTF zeros on the unit circle.

We consider even-order (2n) architectures that allow an odd number of zeros $(2n - 1)$ in the signal band and the remaining zero at the image position. An even number of delay cells from the inputs X_R and X_Q to outputs N_R and N_Q also means an integer number of pairs of delay cells. Therefore, a suitable transformation of the architecture of Fig. 1*a* leads to the scheme of Fig. 1*b* with two delay cells (z^{-2}). The injection at the input of every even cell is delayed and moved to the output. The transformation doubles the time allowed for implementing the delays but requires the availability of delayed intermediate injections.

Let us duplicate the scheme of Fig. 1*b* to make a two-path architecture and use one path for even samples and the other path for odd samples as shown in Fig. 2. The duplication makes the delayed injections of the even path available on the odd path and vice versa. Therefore, as shown in Fig. 2, the delayed terms of Fig. 1*b*, are simply realised by cross-coupling connections between the two paths. Each path needs $N/2$ double-delay cells. Therefore the overall scheme requires 2N double delay cells, the same number of single delay cells used in Fig. 1*a*. However, doubling the delay period grants a reduction of the power of opamps by a factor of four.

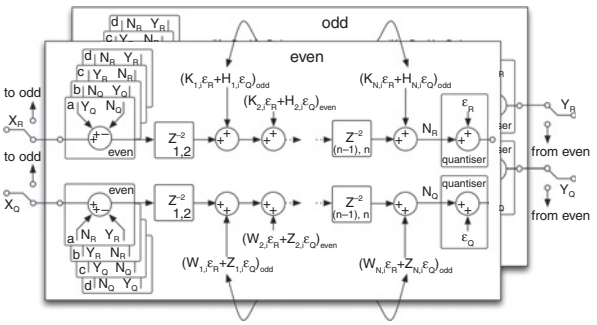

Fig. 2 *Two-path, even-order modulator with double delay cells*

The error analysis given in [4] applies to the schemes of Figs. 1 and 2. An error in the K_i and W_i coefficients shifts the NTF zeros. The shift is limited and zeros remain very close to the unit circle for typical mismatches of modern technology. A mismatch between the R and Q paths gives rise to a spur at the image frequency but this is what also happens in conventional quadrature ΣΔ schemes. A mismatch between the even and the odd paths of Fig. 2 also gives rise to a spur at the image frequency caused by R and Q mismatch. Offset mismatch causes an offset and a tone at $f_S/2$.

Switched capacitor implementation: An opamp and switched capacitor structures implement the two-delay cell and the input and output injection branches depicted in Fig. 3*a*. Fig. 3*b* shows the phase diagram and Fig. 3*c* the circuit schematic. The scheme refers to an output on the even path. A similar scheme holds for outputs on the odd path. There are two inputs V_{1_even}, supposed the main signal, and V_{2_even}. The V_{3_odd}, coming from the other path, is added to the output of the delay cell. The input signals use two switched capacitor structures working in an alternate fashion. One samples the input, the other performs the operation. Therefore, it is necessary to use two phases Φ_{EA} and Φ_{EB} and, for the odd path, Φ_{OA} and Φ_{OB}, respectively. A single switched capacitor scheme implements the addition of V_{3_odd}. The capacitors implementing the main signal flip around the opamp to optimise the feedback factor and limit the slewing requests. A similar scheme is used for the R and Q and the even and odd paths. Capacitors C are nominally equal with a value that matches the KT/C limitation. A possible

mismatch between the two implementing the input terms gives rise to a modulation at $f_S/4$. The spur tones are typically far away from of the signal band and its image. Notice that the circuit of Fig. 3*c* does not compensate for the opamp offset, which is, actually, not needed because of the bandpass response of the entire modulator.

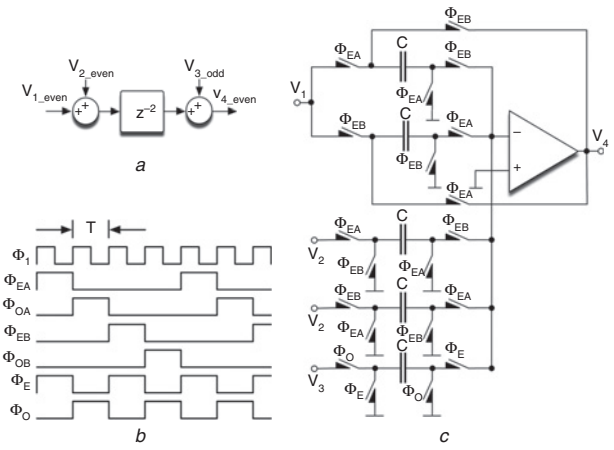

Fig. 3 *Basic double delay cell, clock phases and switched capacitor implementation*

a Basic double delay cell
b Clock phases
c Switched capacitor implementation

The scheme of Fig. 3 gives rise to another possible benefit. Since it requires the opamp during the even periods it is possible to share the same opamp for the active operation of even and odd periods. The delay line architecture and the flip around arrangement fully cancel the memory of previous signals and do not require increasing bandwidth and slew-rate of opamps. The result is that the scheme uses only N opamps for the entire architecture, granting an extra reduction of active area and power consumption by a factor two. Simulation results at the behavioural level with functional and circuit simulators fully verify the effectiveness of the method. Fig. 4 shows a typical resulting spectrum with a random mismatch between coefficients of 0.3%. The noise floor in the IF band is as good as the ideal case. The image tone is as low as -60 dB_{FS} and other tones are below -70 dB_{FS}.

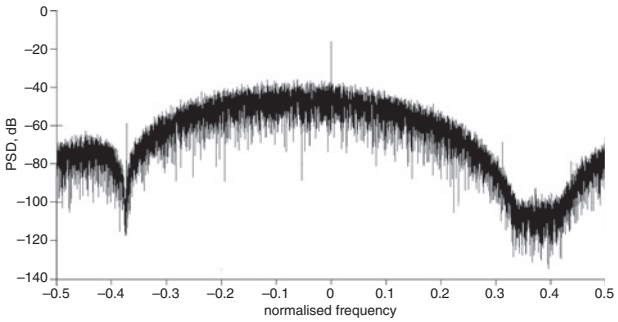

Fig. 4 *Output spectrum with 0.3% coefficient mismatch*

Conclusion: This Letter describes a two-path delay based scheme for a quadrature ΣΔ modulator. The modulator is flexible since simply tuning the sampling frequency scales IF and noise shaping. The IF is mismatch insensitive being locked to the clock. A proper two-path circuit implementation allows significant power saving.

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