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# Exact design of continuous-time sigma-delta modulators with multiple feedback DACs

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**Abstract** A technique for the exact design of the noise transfer function of Continuous-Time (CT) Sigma-Delta modulators with arbitrary and multiple DAC responses and real op-amps is here presented. The approach, that presupposes linear behavior of active blocks, produces a CT modulator with the same noise shaping as its Discrete-Time counterpart. The method operates entirely in the time domain and accounts for non-idealities of real implementations such as finite gain and bandwidth of integrators. The procedure can be effectively implemented with circuit simulators to allow the exact design with transistor level blocks. A design example on a third-order scheme confirms the effectiveness of the method.

**Keywords** Analog to digital conversion · Sigma delta modulation · Continuous-time systems · Sampled data systems

## 1 Introduction

Continuous-time (CT) ΣΔ modulators are effective alternatives to Discrete-time (DT) schemes for medium resolution, large signal bandwidth and low power. The key difference between a CT and a DT architecture is in the position of the sample and hold (S/H), [1, 2]. It is just before the quantizer in the CT schemes while in the DT version sampling is outside the loop (Fig. 1).

Having the sampler inside the loop complicates the design because time transients influence the operation. For a sampled-data scheme what matters is the signal at the sampling times, $T_S$, at the end of possible transients. On the other hand, the signal in front of the S/H at the sampling times of CT integrations depends on details of transients, namely multiple integrations of the input and of the impulse response of the digital to analog converters (DACs).

Established design methods give rise to a CT modulator starting from a sampled-data prototype with almost the expected performances. Conceptually, the loop transfer function of the DT modulator $H_D(z)$, shown in Fig. 1(a), determines the CT counterpart of Fig. 1(b) by using the processing function $H_C(s)$ and the DAC response, $H_{DAC}(s)$. They determine the CT loop transfer function in the Laplace domain

$$G_C(s) = H_C(s) \cdot H_{DAC}(s) \tag{1}$$

to give rise to the equivalence condition linking the DT and the CT loop equations

$$\mathcal{Z}^{-1}\{H_D(z)\} = \mathcal{L}^{-1}\{H_C(s) \cdot H_{DAC}(s)\}|_{t=nTs}. \tag{2}$$

Earlier publications resolve (2) with different mathematical approaches, like the modified $z$ transform [3], the impulse invariant method [4], the state-state approach [5, 6], the s-domain approach [7] or numerical optimization [8]. For the DAC response, these methods typically use a zero-order interpolator or a rectangle lasting a fraction of the clock period. Other more complex DAC responses and limits like the finite gain bandwidth of active blocks are difficult to study.

Indeed, the DT–CT transformation does not give rise to a single feedback path as shown in Fig. 1(b). There are

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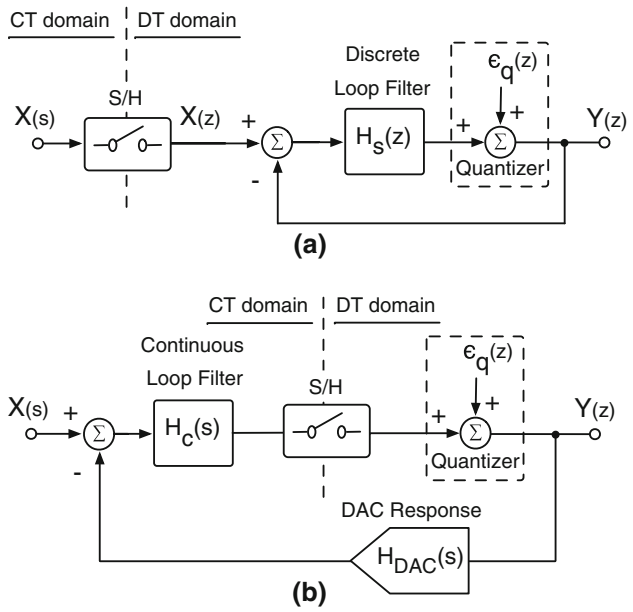


**Fig. 1** Linear model of a discrete-time ΣΔ (**a**) and of a continuous-time (**b**) ΣΔ modulator

always additional branches toward the inputs of intermediate integrators that make the CT architecture a multiple feedback DACs scheme. Obviously, differences in the impulse responses of the DACs influence performance. Moreover, use of different impulse responses may be required, but current design methods can account for this option only by successive manual adjustments [9].

The method proposed here allows an exact equivalence of the NTF response of a CT design and its DT prototype. The approach operates entirely in the time-domain, allows different impulse responses of multiple DACs and accounts for non idealities of building blocks, even when described at the transistor level. The only obvious requirement is that the impulse response vanishes within one clock period. Otherwise, it would be necessary to start from DT prototypes with FIR filters in the loop or to use the approximate methods that correct the limit caused by the excess loop delay, [4].

## 2 Limits of CT design methods

A DT prototype gives rise to a CT equivalent by replacing sampled data integrators with CT integrators. The time constants on the signal path are unchanged while the coefficients in the branches that feed back the digital output change depending on the impulse DAC responses ($h_i(t)$). The reason is that differences in the operation of a DT and a CT integrator propagate through the cascade making it necessary to perform correcting actions along the architecture.

Consider, for example, Fig. 2. It is a multiple chain of $k$ discrete integrators with distributed feedback. Conceptual schemes use a single DAC and local amplification to realize the $\beta_i$ design coefficients. Real implementations use separate DACs typically made by binary weighted or unary capacitors with suitable unity value.

The design methods that transform the DT prototype into a CT equivalent determine the feedback coefficients $\omega_{i,j}$. The first index refers to the position of the DAC in the DT scheme. The second index indicates the injection position in the CT counterpart. The $\omega_{i,j}$ coefficients depend on the impulse response of the DAC. The conventional DT–CT transformation methods proposed in the literature presuppose using a DAC with equal impulse response along the cascade.

Therefore, in the case of different DAC impulse responses, the correct implementation of a multi-feedback scheme is the one in Fig. 3. The injection in position 2 is the superposition of the impulse response of DAC1 multiplied by $\omega_{1,2}$ with the impulse response of DAC2 multiplied by $\omega_{2,2}$. For the injection in position 3 there are three terms injected with the impulse response of the first, second and third DAC and so forth for the successive inputs.

Since the use of many DACs as required by Fig. 3 is unpractical, real implementations normally approximate the design by adding the design coefficients and implementing the superposition with the DAC used at that input. With significant differences between the DAC responses the error is not negligible.

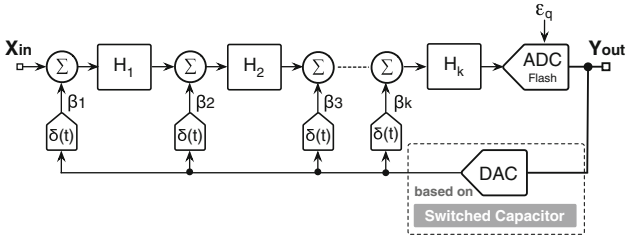


**Fig. 2** Generic $k$-th order discrete time ΣΔ modulator

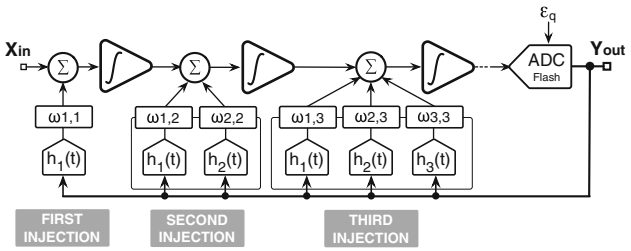


**Fig. 3** Equivalent CT ΣΔ modulator with multiple DAC responses

## 3 Time equivalent exact design

The goal of this study is to make the NTF of the continuous time scheme equal to the NTF of the DT prototype. The STFs do not match because having equal STFs is not particularly relevant, being enough to have the same signal responses in the signal band and alike responses outside signal band.

The method studied here states that equal NTFs result from a CT and a DT schemes that are exact equivalents, a property for which all the samples of the DT and the ones of the CT taken at the sampling times, as used to drive the analog to digital converters (ADCs), are equal for any DAC input sequence and zero input signal. If the circuits are exactly equivalent, the processing of the quantization noise within the quantization loop gives rise to the same sampled data responses.

The design of exactly equivalent modulators is conveniently done in the time domain. For the sake of simplicity, we illustrate the method starting from a third order low-pass DT prototype, as shown in Fig. 4. The extension to higher order or other architectures is not difficult. The DT integrators are accumulators ($A_{CCUi}$) with impulse response $h_i(nT)$. The accumulators could be with or without delay, but in every feedback loop it is necessary to have at least one delay. The feedback coefficients, $\beta_1$, $\beta_2$, $\beta_3$ and the possible delay of the sampled-data integrator produce the DT signal and noise transfer functions. How to derive coefficients and how to possibly assign delay to integrators is known, [1], but not discussed here.

The first step of the procedure is to expand the scheme into branches made of the cascades of integrators. The result is shown in Fig. 5. The second and the third integrators are duplicated to give rise to separate processing; the outputs of the branches are summed up to determine the input of the quantizer. Notice that each branch processes only signals coming from the DAC, the input of the modulator being set to zero. The linear property of the scheme ensures the correspondence between Figs. 4 and 5. Therefore, $P_Q(nT)$, the input of the quantizer, is $P_Q(nT) = P_1^3(nT) + P_2^3(nT) + P_3^3(nT)$.

Thanks to the linear property, the exact CT equivalent of Fig. 4 must be also the exact equivalence of Fig. 5.

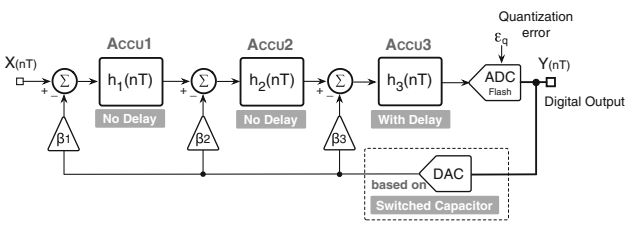


**Fig. 4** Discrete time third order low pass ΣΔ modulator

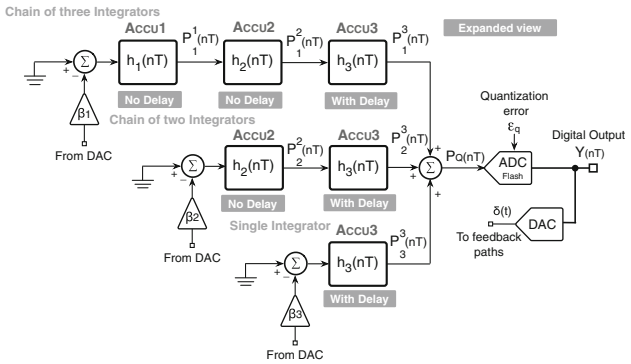


**Fig. 5** Expanded view of a discrete time third order low pass ΣΔ modulator

Therefore, it is required to find the exact equivalence of each branch of the expanded scheme. We will see that the CT exact equivalent of a branch with multiple integrators needs extra injection of CT signals. This must be done through DACs whose impulse response is the one of the converter used on that intermediate input.

The superposition of exact equivalent branches gives rise to the overall CT architecture. The result has the same architecture as in Fig. 4, with CT integrators replacing the sampled data counterpart but, obviously, the CT feedback coefficients are different. The study assumes, as normally done in CT designs, that CT integrators have a time constant equal to the sampling period.

The exact equivalence must hold for any waveform delivered by the Flash ADC; however, since the system is linear, it is possible to focus the study on a delta pulse driving the DT and the CT DACs. For the DT scheme, the DACs have delta at output. The CT schemes use the impulse responses of the DACs. As already mentioned, they can have any waveform, but it is assumed they go to zero at the end of the sampling period. Otherwise, the impulse response should be divided into two sections with the second one entered during the next clock period. That would correspond to the presence of a transversal filter in the DT prototype.

### 3.1 Single integrator exact equivalence

Figure 6 shows the bottom DT branch of Fig. 5 and its CT counterpart. The sampled data accumulator is with delay because it is the only block around the loop, just before the quantizer. For the CT architecture the input of the integrator is the impulse response of the DAC. Notice that, at the beginning of the clock period, a small fraction of time-slot is dedicated to the quantization process.

Normalizing the time of the sampling period $T_S$ to 1, the output of the DT integrator is

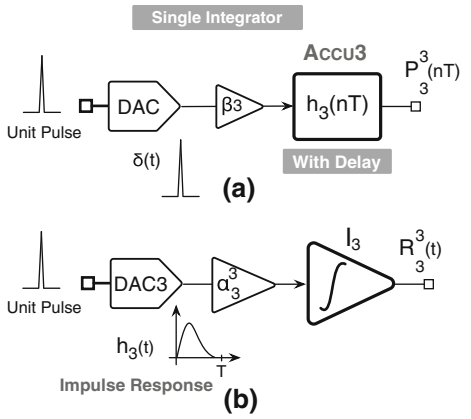


**Fig. 6** Discrete (**a**) and **b** continuous time single integrator branch

$$P_3^3(n) = \beta_3 step(n-1) \tag{3}$$

The output of the CT integrator is

$$\begin{cases} R_3^3(1) = \alpha_3^3 \int_0^1 h_3(\tau)d\tau & t \le 1 \\ R_3^3(n) = \alpha_3^3 \int_0^1 h_3(\tau)d\tau & n > 1. \end{cases} \tag{4}$$

where $h_3(t)$ is the impulse response of DAC3.

The time equivalence conditions lead to

$$\beta_3 = \alpha_3^3 \int_0^1 h_3(\tau)d\tau = \alpha_3^3 h_{int,3}^1 \tag{5}$$

that defines $h_{int,3}^1$, the first integral of the DAC3 response, $h_3(t)$, over the sampling period.

Notice that the shape of the waveform of the CT outputs within the [0, 1] period is irrelevant; what matters is its value at the sampling times $t = n$. Moreover, since the DAC control is a single pulse $\delta(t)$, the DT and CT outputs remain constant for $n > 1$. Having equal outputs at $t = 1$ ensures that the outputs are equal for any time $t = n > 1$.

### 3.2 Double integrator exact equivalence

For the cascade of two DT integrators there are two different options: first integrator without delay, as shown in Fig. 7(a) or first integrator with delay. Let us consider the former case first. With a $\delta(t)$ pulse at input the output of the first integrator is a step and that of the second integrator is a staircase with values at the sampling times $t = n$ given by

$$\begin{cases} P_2^2(n) = \beta_2 step(n); \\ P_2^3(n) = \beta_2 \cdot n \quad n > 0. \end{cases} \tag{6}$$

The CT counterpart must be able to generate the same amplitude at the output of the second integrator at time $t = 1$ and give rise to a ramp with the same slope for $t > 1$. Since the slope depends on the output of the first integrator at $t = 1$ it is necessary to meet two conditions and this, according to a simple verification, cannot be realized with one parameter.

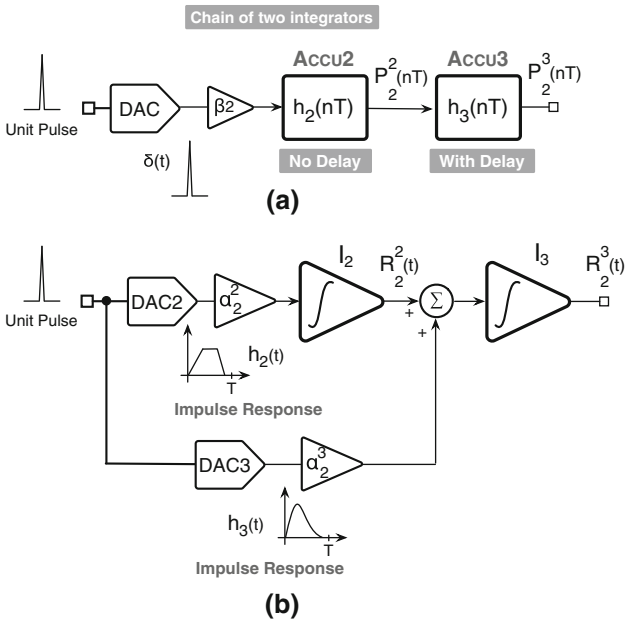


**Fig. 7** Chain of two integrators: discrete (**a**) and **b** continuous time version

It is necessary to plan for two injections at the input of the first and the second integrator. The injection onto the second integrator must match the impulse response of DAC3. The request on equal slopes determines the gain factor, $\alpha_2^2$. The condition on equal outputs gives rise to the coefficient $\alpha_2^3$, of Fig. 7(b).

The exact equivalent conditions are

$$\begin{cases} P_2^2(1) = R_2^2(1); \quad \beta_2 = \alpha_2^2 h_{int,2}^1; \\ P_2^3(1) = R_2^3(1); \quad \beta_2 = \alpha_2^2 h_{int,2}^2 + \alpha_2^3 h_{int,3}^1 \end{cases} \tag{7}$$

where

$$h_{int,2}^1 = \int_0^1 h_2(\tau)d\tau \tag{8}$$

$$h_{int,2}^2 = \int_0^1 h_{int,2}^1(\tau)d\tau, \tag{9}$$

are the first and second integrals of the DAC2 response over the [0, 1] time interval.

The case of two DT integrators with delay determines the following DT impulse responses

$$\begin{cases} P_2^2(n) = \beta_2 step(n-1); \\ P_2^3(n) = \beta_2 \cdot n \quad n > 1. \end{cases} \tag{10}$$

The condition on the slope remains unchanged because it holds for $t > 1$. The exact equivalent conditions are

$$\begin{cases} P_2^2(1) = R_2^2(1); & \beta_2 = \alpha_2^2 h_{int,2}^1; \\ P_2^3(1) = R_2^3(1); & 0 = \alpha_2^2 h_{int,2}^2 + \alpha_2^3 h_{int,3}^1 \end{cases} \tag{11}$$

which, again, together with the impulse response of the CT scheme, determine the parameters $\alpha_2^2$ and $\alpha_2^3$ which ensure exact equivalence.

Another procedure that gives rise to exact equivalence is to use the conditions that are verified if values and slopes are equal at t = 1.

$$\begin{cases} P_2^3(1) = R_2^3(1) \\ P_2^3(2) = R_2^3(2), \end{cases} \tag{12}$$

Their extensions are more convenient conditions for high order schemes.

### 3.3 Triple integrator exact equivalence

The branch of three DT integrators with or without delay has $\beta_1$ as input multiplier of the input DAC. The injection of a pulse gives rise to DT second order ramps with the delay established by the architecture at the output. For example, three integrators and only one delay in the last stage, like the one shown in Fig. 8(a), and a pulse at input give rise to

$$P_3^3(n) = \beta_3 \sum_1^n \sum_0^n 1. \tag{13}$$

The CT architecture that enables exact equivalence is the one in Fig. 8(b). The outputs $R_3^3(n)$ at times $t = 1, 2, 3$ are

$$\begin{cases} R_3^3(1) = \alpha_1^1 h_{int,1}^3 + \alpha_1^2 h_{int,2}^2 + \alpha_1^3 h_{int,3}^1 \\ R_3^3(2) = R_3^3(1) + \alpha_1^1 h_{int,1}^2 + \alpha_1^2 h_{int,2}^2 \\ R_3^3(3) = R_3^3(2) + \alpha_1^1 (h_{int,1}^1 + h_{int,1}^2) + \alpha_1^2 h_{int,2}^2. \end{cases} \tag{14}$$

The exact design condition requires $P_3^3(1) = R_3^3(1)$, equal slope and equal second order derivative or, equivalently

$$\begin{cases} P_3^3(1) = R_3^3(1) \\ P_3^3(2) = R_3^3(2) \\ P_3^3(3) = R_3^3(3); \end{cases} \tag{15}$$

that make a linear system of three equations needed for estimating the design parameters $\alpha_1^3$, $\alpha_2^3$ and $\alpha_3^3$.

### 3.4 Superposition of results

The exact equivalences of the three branches of Fig. 5 determine three schemes that involve one DAC injection at the input of the first integrator, two DAC injections at the input of the second integrator and three DAC injections at the input of the last integrator. Since the DACs of the CT exact equivalent have the same impulse response it is possible to superpose their effects, leading to the scheme of Fig. 9. The $\alpha_i$ coefficients are

$$\begin{cases} \alpha_1 = \alpha_1^1 \\ \alpha_2 = \alpha_2^1 + \alpha_2^2 \\ \alpha_3 = \alpha_3^1 + \alpha_3^2 + \alpha_3^3. \end{cases} \tag{16}$$

Thus obtaining the exact equivalence in the time domain allows one to equal the input at the quantizer in both modulators at each sampling time. This provides the same processing as the feedback loop and consequently the same NTF for both modulators.

### 3.5 Extension to higher order

The design methodology developed for the third order scheme can be extended to higher order modulators with low-pass or band-pass response. The design steps are the same. They are summarized as follows:

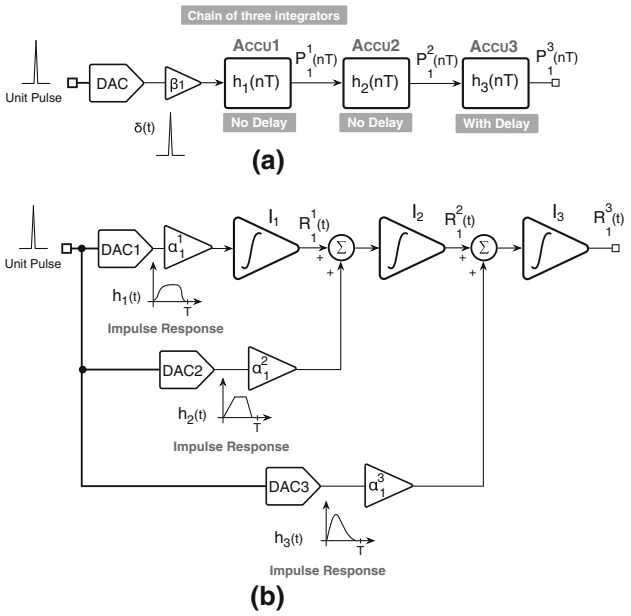


**Fig. 8** Chain of three integrators: discrete (**a**) and **b** continuous time version

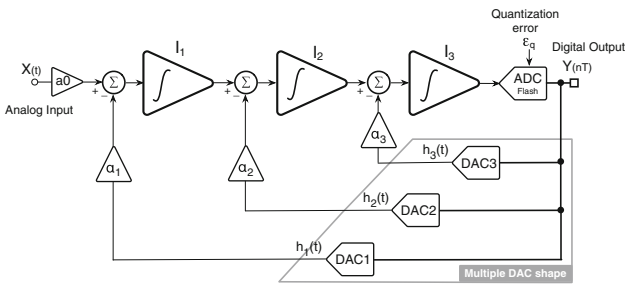


**Fig. 9** Continuous time final block diagram

- Define the DT prototype and consider only the paths from the ADC.
- Expand the DT prototype into parallel processing. Duplicating the DT integrator gives the quantizer input as the superposition of paths made by a cascade of integrators without intermediate inputs.
- Obtain the DT–CT exact equivalence of each branch by estimating the output responses of a DT and a CT counterpart with multiple intermediate inputs. The DAC of the intermediate input must have the impulse response of the DAC used in the final scheme in that position.
- Resolve the system of linear equations that make the outputs of the DT and CT branches equal at times $t = 1, 2, \cdots N$, where $N$ is the number of integrators of the branch.
- Superpose the exact equivalent of branches to produce the final architecture.

## 4 Nonidealities in CT ΣΔ Modulators

The loop filter of a CT ΣΔ modulator determines the noise transfer function and thereby the quantization noise-shaping behavior. However, any source of non-idealities directly affect the performance of the CT modulator by increasing the integrated in-band noise which causes a degradation in the final SNR.

Among these non-idealities there is the finite operational amplifier's gain $A_{dc}$. This limit affects both low-pass CT and DT modulators since the zeros of the NTF are pushed inside the unity circle, thus reducing quantization noise attenuation in the signal band. Fortunately, for medium resolution the required gain is well affordable so that the limit is not normally a real concern. Other sources of errors are the finite gain-bandwidth product (GBW) and the slew-rate of active blocks used for the integrators. The slew-rate limit mainly affects the DT modulators. Indeed, low slew-rate sensitivity mainly motivates the choice of CT architectures; the signal injected at the feedback input lasts for a large fraction of the sampling period, thus reducing the op-amp peak output current and its derivative.

The finite GBW is the most critical limit for the CT schemes because it delays the transfer of the input signal to the output of single or multiple real integrators [10].

Consider, for example the cascade of a DAC with one and two integrators as shown in Fig. 10. The outputs with real op-amps obviously differ from the ones with ideal op-amps and this degrades performance. However, it is possible to incorporate the bandwidth limit into the DAC response. For this it is necessary to pass the output waveform of the real integrator(s) through one or more derivations

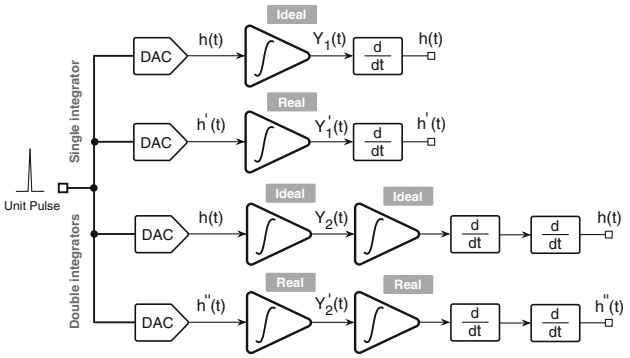


**Fig. 10** Procedure that allows determining the input referred equivalent DAC impulse response for single and double integrators

(ideal). The result of the operation is an input referred equivalent DAC impulse response ($h'(t)$ or $h''(t)$) that, used with ideal integrators, would determine the same output of the real integrator counterpart. Fig. 11 shows a possible DAC input response and its input referred equivalents for the cascade of one or two integrators and two different op-amp bandwidths ($GBW_1 = 2f_S$ and $GBW_2 = 3f_S$). These results are obtained by using a behavioral description of integrators. Notice that there is a delay that increases as the bandwidth decreases and is larger for a cascade of multiple integrators. The results depicted in Fig. 11 recommend anticipating the fall time of the DAC responses injected at the beginning of integrator chain in order to avoid a tail in the next clock period. This method obviously requires accounting for different DAC impulse responses as with the method discussed in this paper.

Remember that the design procedure requires estimating multiple integrals of the DAC response. For a real integrator it would be necessary to estimate the input referred DAC response before and to pass that waveform through a single or a multiple ideal integration. Since the estimation of the input referred DAC response includes derivatives, the following ideal integrations compensate for them. Therefore, the needed parameters $h^j_{int,i}$ are conveniently estimated by passing the actual DAC response through real integrators instead of taking the mathematical integration of the input referred impulse response. The operation can be done with a circuit simulator that uses the transistor-level description of the used op-amp.

## 5 Design example

The effectiveness of the design methodology is verified with a 2-bit third order DT ΣΔ modulator whose diagram is shown in Fig. 4. All the feedback coefficients equal to one. With a sampling frequency of 200 MHz and an OSR of

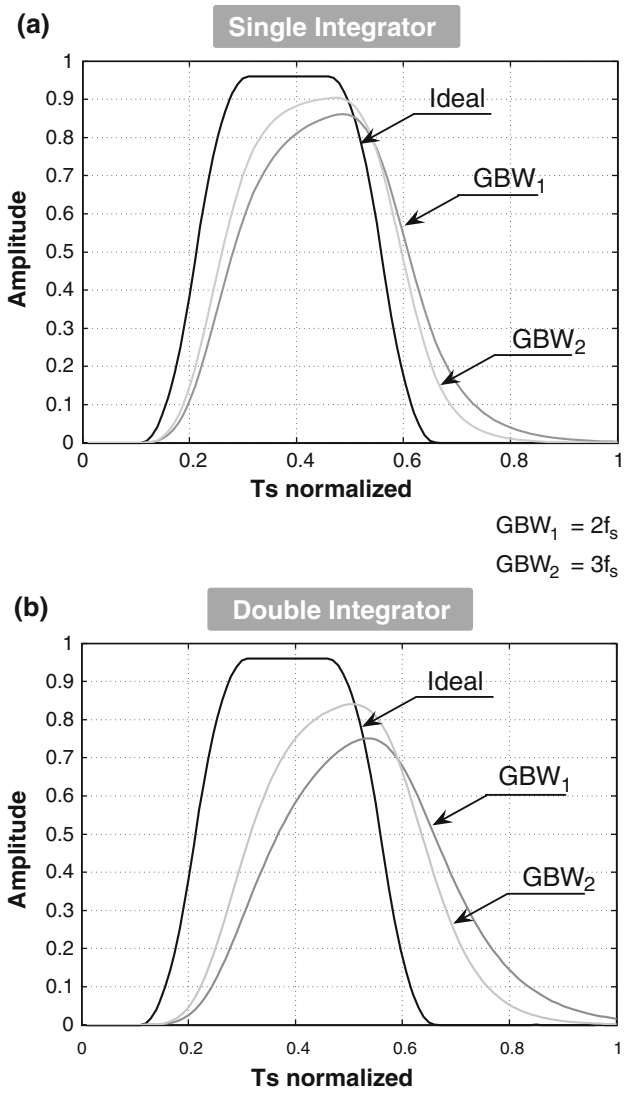


**Fig. 11** Effects of finite GBW on input referred DAC response: **a** single integrator and **b** double integrators

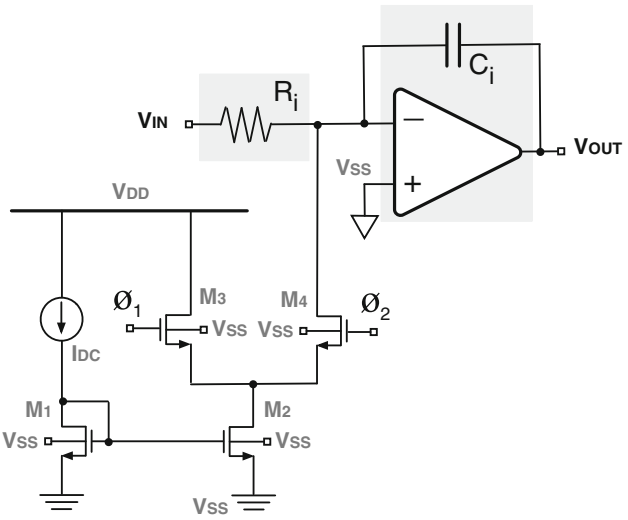


**Fig. 12** Implementation of a current feedback DAC with active RC integrator

16, the effective number of bits (ENOB) is 12.09. The equivalent CT architecture uses active RC integrators and current feedback DACs whose basic cell is the scheme of Fig. 12. The use of a clock with rise and fall times as low as 100 ps gives rise to the current switching without significant delay. This feature has been verified with simulations at the transistor level with a 65-nm CMOS technology for the DAC scheme and a behavioral description of the amplifier. However, a real op-amp is not able to keep virtually shorted the differential inputs. Thus, the amount of charge injected into the virtual ground and the output waveform depend on the op-amp features and not on the DAC scheme. With an ideal op-amp the output voltage is a ramp determined by current, capacitance $C_i$ and pulse duration. However, with real circuits, non-idealities such as finite gain and bandwidth of operational amplifiers alter the output waveform. Notice that it is possible to give rise to the same output waveform with an ideal op-amp and an input-referred DAC response estimated by the time derivative of the real output signal. The area of the input referred DAC response is lower than the one of the ideal case because the virtual ground experiences a voltage transient.

For the cascade of two or more real integrators the output of the last op-amp accounts for the limits of the real blocks used. Even in those cases we can define an input referred DAC response that gives the same output with ideal integrators. The above study, done at the transistor or behavioral level, provides the coefficients necessary for the exact design but, in addition, gives indications on the possible return-to-zero timing that avoids the excess loop delay.

Suppose using an op-amp with 60 dB DC gain and the single-pole bandwidth limitation. Figure 13 shows the simulated waveforms of the input referred DAC response for different values of GBW ($2f_S$, $3f_S$, and $4f_S$), together with the case of an almost ideal op-amp (gain = 100 dB and GBW = $8f_S$). These results are obtained by using a behavioral description of the amplifier. The figures refer to the cascade of one, two and three integrators, respectively. The clock of the DAC has an arbitrary RTZ (from 10 to 60% of the clock period). Results show a tail and a delay in the input referred DAC response. Both increase as the bandwidth decreases and are larger for the cascade of multiple integrators. Since for GBW = $2f_S$ and a cascade of three integrators the tail extends the sampling time, it is a good practice using a GBW that is at least $3f_S$. The input referred responses with two or a single integrator behave

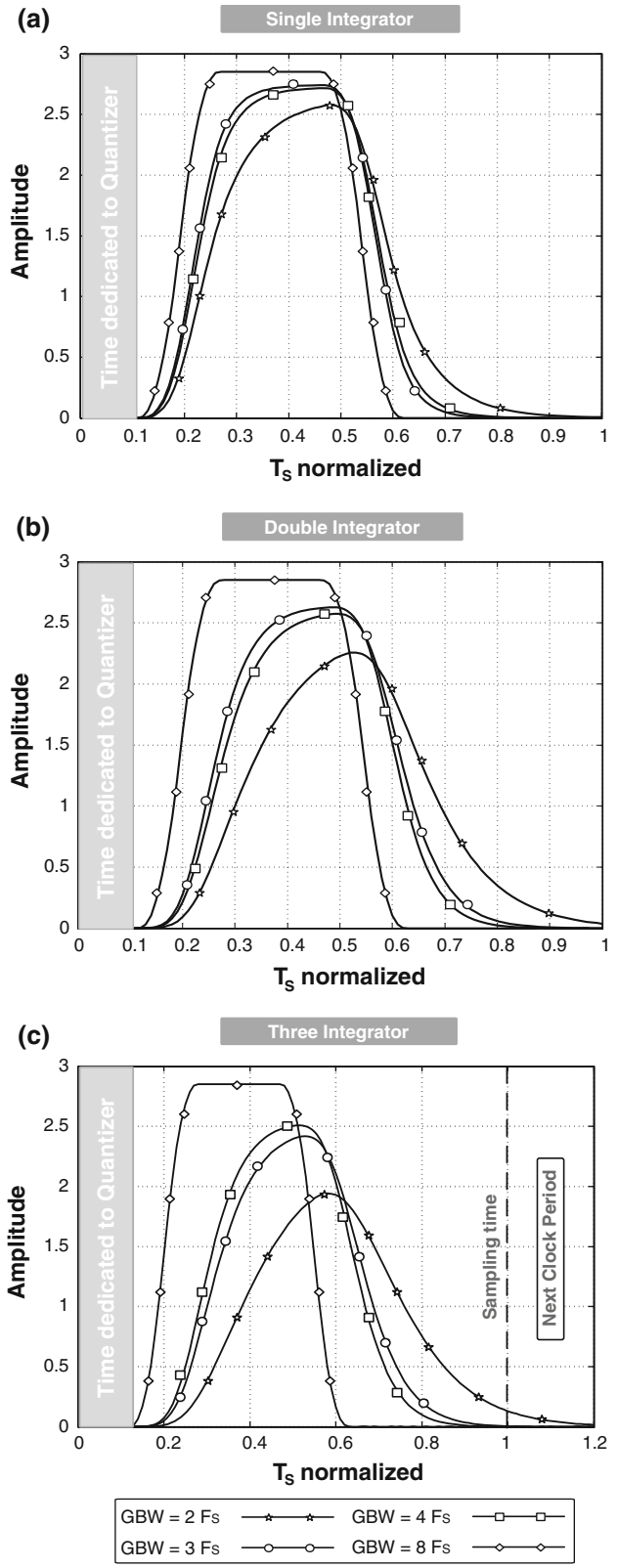


**Fig. 13** Input referred equivalent DAC1 impulse response with finite GBW and a gain of 60 dB (the curve with GBW $= 8f_S$ uses a gain of 100 dB): **a** single Integrator. **b** double integrator. **c** Three integrators

**Table 1** Coefficients for a third order ΣΔ Modulator: CT-1 uses integrators with GBW $= 8f_S$ and 100 dB gain, CT-2 uses integrators with GBW $= 3f_S$ and 60 dB gain

| DT | Value | CT-1 | Value | CT-2 | Value |
|---|---|---|---|---|---|
| $\beta_1$ | 1 | $\alpha_1$ | 2.85 | $\alpha_1$ | 2.99 |
| $\beta_2$ | 1 | $\alpha_2$ | 4.11 | $\alpha_2$ | 4.56 |
| $\beta_3$ | 1 | $\alpha_3$ | 2.78 | $\alpha_3$ | 3.32 |

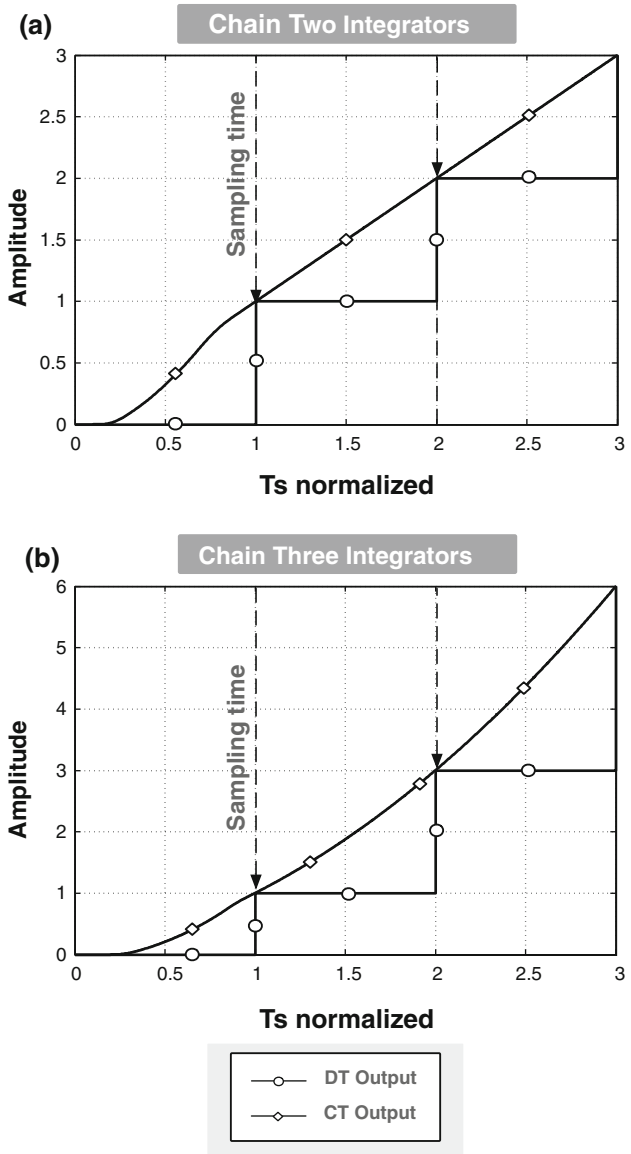


**Fig. 14** Impulse response DT–CT equivalence: **a** chain of two integrators, **b** chain of three integrators

better. Supposing to use a GBW equal to $3f_S$, the pulse vanishes at 0.85T and 0.75T. Thus, the return to zero of the corresponding DACs can occur at delayed times: 0.75T and

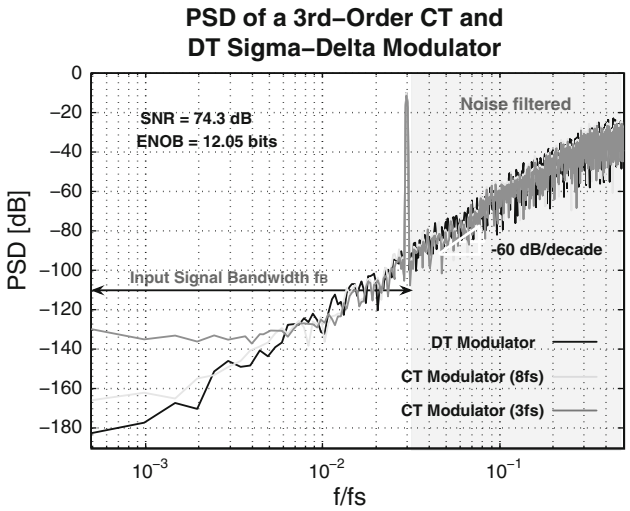


**Fig. 15** Simulated output spectrum of the third order multi-bit DT modulator and its equivalent CT implementation (OSR = 16). FFT with 4,096 points

0.85T, respectively, with a consequent reduction of the bias current of the DAC and, consequently, the one of the op-amp.

The use of the optimal duty-cycles in the behavioral simulation provides the results needed for the exact design performed following the above described procedure. Table 1 resumes the list of the coefficients obtained for CT and DT modulators with an ideal and the real CT integrators. The waveforms of the CT circuit in the time domain perfectly equal the DT counterparts at sampling times either with ideal and real op-amps (Fig. 14 uses CT integrators with GBW = $8f_S$ and gain = 100). Since the quantizer inputs match (Fig. 14) the NTFs also match, as shown in Fig. 15. The simulated output spectra correspond to the DT scheme and the CT implementations designed using the coefficients of Table 1, calculated with the analysis of this paper and the DAC responses of Fig. 13. The FFTs, that use 4096 points, are not exactly superposed because the different signal transfer functions slightly alter the values in the time domain. The spectra perfectly match with zero input. With an input signal at $0.0298f_S$, the SNR is about 74 dB.

## 6 Conclusions

This paper proposes a general methodology that gives rise to an exact equivalence between the NTFs of a DT prototype and its CT counterpart. The method works completely in the time domain, without resorting to the $z$ or $s$ domains. The approach leads to a straightforward design and allows any DAC waveform. Moreover, the tuning of the design coefficients that compensate for the limited GBW of operational amplifiers is possible.

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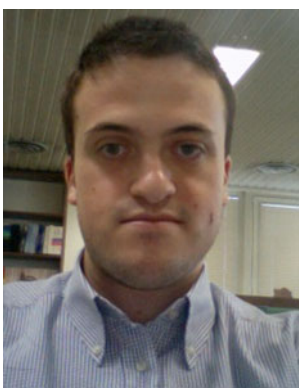

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