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Optimum selection of capacitive array for multibit Sigma-Delta modulators without DEM

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Abstract A method for a smart selection and sequencing of unity capacitors in a multibit digital-to-analog converter (DAC) that improves the linearity is proposed. The approach, suitable for the DAC nonlinearity correction in Sigma-Delta modulators, obtains better results than dynamic element matching. The key of the proposed technique is an off-line self-measurement of mismatches with the available hardware. The results significantly improve when redundant DAC capacitors are introduced. Hence, the capacitors are selected from a set that is larger than required. An affordable silicon area overhead introduced by the redundant capacitors avoids extra power consumption, that is unavoidable in other methods during the normal operation of the converter.

Keywords Sigma Delta · Multi-bit · DAC linearity

1 Introduction

Recent applications require analog-to-digital converters (ADCs) with medium-to-high resolution and very high operation speed. The challenges introduced by those applications to ADCs push them to their performance limits, asking for new innovative methods to obtain high performance with reduced power consumption. Considering such constraints introduced by the applications, the use of multi-bit Sigma-Delta (ΣΔ) ADC's [1] is generally a preferred strategy. However, this choice may sometimes be not appealing to the designers as it introduces strict linearity constraints on the DAC. Hence, techniques to improve this linearity can allow designers to take advantage of multi-bit ΣΔ-ADCs in their designs for recent performance demanding applications.

There are many design dimensions in order to increase the resolution of ΣΔ-ADCs [2–4]. Among them, there are the order of the modulator and the oversampling ratio, normally pushed to the limits for the best performance. Furthermore, having better resolution in the DAC increases the overall resolution even if, as mentioned, the linearity of the multi-bit DAC becomes a critical design parameter. In order to overcome this bottleneck, calibration and trimming methods were introduced. However, these methods add overhead to the system during conversion, thus increasing the overall power consumption. In addition, some of these methods use blind averaging disregarding the typical characteristics of error which can be measured. Hence, such blind approaches prevent the calibration techniques from achieving the best attainable solution.

One well known approach for increasing the linearity of multi-bit DAC is the dynamic elements matching (DEM) [2] method that scrambles or sequentially uses the unity elements of the DAC. According to a given algorithm, DEM eventually shapes the noise coming from the mismatch error. However, error is not reduced but only transformed into a pseudo-noise spread over the spectrum leading to a possible source of tones in the signal band.

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Moreover, the required logic circuitry operates at the oversampled frequency, increasing the power consumption and reducing the effectiveness of the converter. One relevant aspect of DEM is that it is a digital technique which operates without any knowledge of mismatch-error [3]. Hence, the error is averaged blindly, without measuring the mismatch. Another popular choice is to use data weighted averaging (DWA) which shapes the noise [4]. However, DWA suffers from in-band tones which cannot be avoided. Although there are other advanced methods proposed earlier in the literature that improve the performance of the DAC, none of them (including DEM and DWA) can be implemented without degrading the SNR [5]. There are also other approaches for current steering DACs [6] which take advantage of redundant transistors to calibrate to the desired value. This method takes advantage of similar principle to the one proposed but requires extra circuitry for measurement and calibration phase.

This work exploits the possibility offered by the ΣΔ modulator to perform a preliminary measure of the value of unity elements used in the DAC with the available hardware. Our method [7] uses this measurement information for a smart selection of elements, thus avoiding DEM, while obtaining excellent performances. In addition, the method is independent from the oversampling ratio which is an important advantage, especially considering DWA based methods. In the following sections the proposed approach is described. In Sect. 3, the error measurement and selection method of the capacitors is presented. The optimum selection and the effects of increasing the capacitors number are explained in Sect. 4, while the simulation results are reported in Sect. 5 The last section concludes the paper.

2 Proposed method

There are many DAC structures that can be preferred depending on the application and specifications of the ADC. Capacitor based DACs are generally preferred for various applications [1]. The capacitor DAC used in ΣΔ modulator is formed by a set of N unity capacitors, C_u, nominally equal, thus providing a linear characteristic in ideal case. However due to process variations, the mismatch among them makes each unit capacitor deviate from its ideal value as given in (1):

$$C_i = C_u + \varepsilon_i \tag{1}$$

The sequence of errors ε_i has a systematic and random component deviating the transfer characteristic of the DAC from its ideal linear behavior. The DEM technique transforms this error into a pseudo-noise whose input referred voltage power is

$$V_{n,\varepsilon}^2 = \frac{V_R^2}{C_{u^2}} \sum_{i=1}^{N} \varepsilon_i^2, \tag{2}$$

where V_R is the DAC voltage reference, C_u is the unit capacitor value, and N is the total number of DAC elements. DEM uses a scrambler circuit which spreads that power uniformly over the Nyquist interval. There are also other methods such as DWA that obtain noise shaping, but however still increasing the in-band noise floor. Therefore they are generally suitable for a σ of mismatch well below 1% and resolutions smaller than 12–14 bit [8–11].

There are some more methods which try to compensate for the deviation by using redundant elements. These elements are much smaller in size, generally the minimum size, and connected in parallel to the element. After the implementation, a calibration phase is required, where these extra elements are activated or not. In most cases, since they are in minimal size, there are more than one of them per unit element. Hence for each unit element one or more of these smaller elements are added depending on the output at the calibration phase. These unit elements can be capacitors or transistors [6], depending on the DAC structure. The main purpose here is to adjust the value of each element to the ideal value as much as possible. However it may be more beneficial to take advantage of the deviation of each element rather than adjusting each one to a desired value as in the case of the proposed method.

Most of methods available in literature, as briefly mentioned above, do not have any information about the mismatch error value but yet perform averaging. Hence they do not eliminate these errors, but try to move around the spectrum whether by spreading or shaping them. However, if the values of the sequence of errors ε_i are known, instead of dynamic use of elements we can consider a "smart" utilization of unity elements to optimize the INL of the DAC. Thus, we can eliminate the apparent error in the DAC rather than moving it around. Assuming to have just a systematic error, the INL may look like as depicted in Fig. 1(a). A proper sequence of the unity elements can change the INL response into the one shown in Fig. 1(b). The behavior in that case will have lower maximum amplitude and more fluctuation around zero.

Notice that the INL of Fig. 1(b) is not a good choice for small input amplitudes in a Nyquist rate DAC but is optimal when the DAC is used in a ΣΔ modulator.

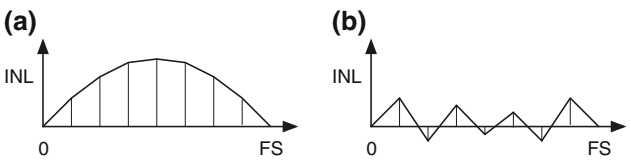

Fig. 1 INL of **a** a systematical error **b** a proper sequence

Digital output that controls the DAC is the input summed with a shaped quantization noise, whose maximum amplitude is the quantization step. Therefore, control of DAC is inherently a dynamic averaging of the DAC levels corresponding to the input amplitude over two or more neighboring quantization intervals. The effect, as verified shortly by computer simulations, is to smooth the effect and to obtain negligible harmonic tones. The proposed method is to use the ΣΔ modulator itself reconfigured as incremental to measure each unity DAC element, and, using this information, to have a capacitors sequence that obtains the INL shown in 1 (b). Knowing the capacitors mismatches it is possible to optimize the DAC linearity by using the capacitor in a proper sequence. However, in case where the available number of unity elements is bigger than what is needed by the DAC, the linearity can be improved further. If the number of available unity elements is the same as needed, there will be still improvement, although limited. The selection can provide much better linearity in the earlier steps of the smart selection process. However, when it comes to last assignments, since the available unity elements which can be selected are fewer, the improvement could be limited. Anyway the number of available unity elements could be larger, meaning there would be redundant capacitors in the design. The level of redundancy can be set by the designer. It may be obvious that, more redundant capacitors would lead better selection hence more linear behavior for the DAC, but even one or two additional capacitors may be sufficient for crucial improvement. For example 9 or 16 capacitors can be placed to be used for the DAC rather than 8 capacitors which are sufficient for a 3-bit DAC. With the redundant capacitors and knowing the mismatch errors, it is possible to choose the most favorable elements for the optimal sequence whether it's an earlier selection or not. This, as verified by simulations, further improves the INL. Hence, the proposed approach provide different levels of accuracy depending on the silicon area that can be allocated for this capacitors and the basic control logic. Please note that these capacitors will be set once and would not change during regular operation hence would not introduce any additional power consumption. As an example, with a 3-bit DAC 16 unit elements can be arranged in a square matrix and the smart selection can use the elements and the sequence of Fig. 2, where a suitable logic determines the capacitances to be used as the sequence.

3 Error measurement

One of the advantages of the proposed method is that, it can take advantage of the available hardware for the calibration phase. Each of the N unit capacitors of the array can be measured off-line using the ΣΔ architecture itself. The structure is re-configured as incremental [12, 13] for this process. The purpose is to utilize only one element at a time. Although the feedback capacitor will also be used, it does not affect the overall measurement since it will be used at each measurement. In the incremental phase the charge stored in two integrators to be used for measurement are being reset at first. A fixed voltage, V_{Meas} lower than V_R/N, where V_R is the DAC reference voltage, is applied to the input of the ADC. The output of the modulator with such configuration is a bit-stream that uses none or just one capacitor only during this process, the one under the measure, C_i. The use of a cascade of integrators (one more than the order of the modulator) provides the digital measure of the input voltage multiplied by the input gain

$$V_{\text{out},i} = C_i \frac{V_{\text{Meas}}}{C_f}. \tag{3}$$

The digital output is the measure of C_i multiplied by an unknown ratio, since C_f, the feedback capacitance in the integrator, is affected by mismatch errors. If the same voltage V_{Meas} is used for the measure with all the unity elements, the results are a relative measure of the values that enables to estimate the mismatches. Then, this knowledge is used for the optimum selection of the unity elements.

With a second order modulator the use of three cascade integrators for K clock periods obtains $K(K+1)(K+2)/6$ as full scale. Therefore, the accuracy of the measurement is approximately $1/(3\log_2 K - 3)$. Therefore by selecting $K = 2^8$ the relative value of each capacitor can be measured with more than 20 bit of accuracy. The elementary scheme to implement the unit capacitor error measurement is shown in Fig. 3, where two controls signals are added:

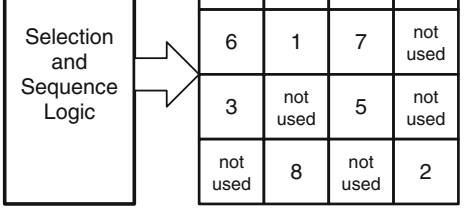

Fig. 2 Layout diagram of a possible capacitor array

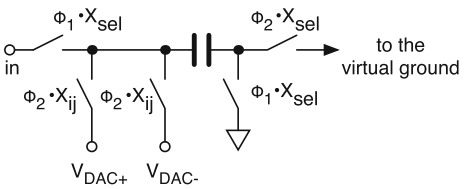

Fig. 3 Switched capacitor scheme of the single unity element

one for the selection, used during the reconfiguration in incremental, and one control for normal operation if the capacitor is selected by the algorithm.

Once the measurement for a capacitor is performed, the set with the best matching is selected. Then, a suitable algorithm for having the minimum INL is performed.

4 Optimum selection

The optimum selection of N elements out of M available corresponds to the set with minimum relative differences. A possible algorithm employs the partial average value $\bar{C}_i$ taken from a set of $(K-1)$ elements that excludes C_i.

$$\bar{C}_i = \frac{1}{K-1}\sum_{j\neq i} C_j. \tag{4}$$

The selections starts with $K = M$ and eliminates the element for which the distance D_i

$$D_i = (C_i - \bar{C}_i)^2 \tag{5}$$

is maximum. Then, $K = M - 1$ and the test continues with eliminations of unit elements one by one until the number of elements required by the DAC is reached.

This choice of the optimal sequence of N elements, $C_1, C_2, \ldots, C_N$, whose average value is $\bar{C} = 1/N \sum C_i$, is performed according to the following algorithm:

The first selected element, $C_{s,1}$ is the one that obtains the minimum value of

$$\Delta_1 = (C_i - \bar{C})^2. \tag{6}$$

The next selected unit capacitor is the element obtaining the minimum

$$\Delta_2 = (C_i + C_{s,1} - 2\bar{C})^2, \tag{7}$$

and so forth. The selected elements of the optimal sequence control a switch matrix that uses the thermometric control of the DAC to provide the logic signals used in the switched capacitor scheme of Fig. 3. Figure 4 shows a possible situation: as a result of each elements measurement, the described algorithm selects the first, third, fourth and the remaining capacitors considering the mismatch errors. The control of the others is grounded by the switches on the top to deactivate these elements. After the assignment process, as presented in Fig. 4, the first capacitor is used to convert the bit T6 of the thermometric signal, the third converts T3 and so forth. Therefore, the circuit overhead is the deactivated elements in the matrix of Fig. 4 and the registers that control the switches. Since the processed signal by the matrix is digital, the use of a switch does not affect, in practice, the speed of operation.

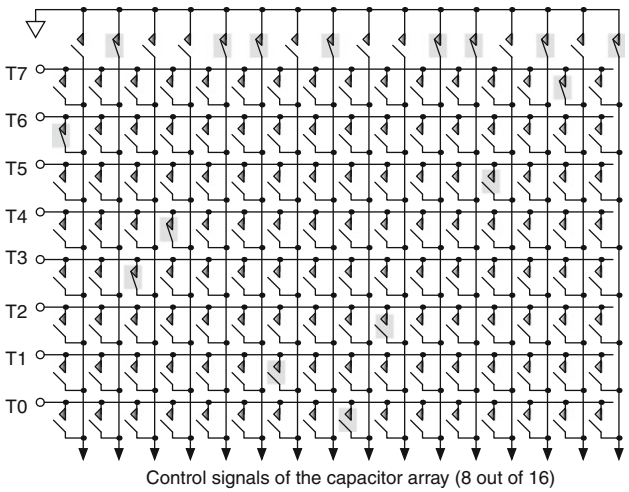

Fig. 4 Matrix of switches suitable for the control of a DAC that uses 8 out of 16 unity elements

5 Simulation results

The proposed approach has been simulated at the behavioral level with various mismatches and signal amplitudes. The first study concerns in the evaluation of the INL in different foreseen cases. Figure 5 shows the statistical distribution of the absolute value of the INL obtained for the case of a 3-bit DAC. The unity capacitances of the DAC have random mismatch value of $\sigma = 0.01$. The distribution concerns 100 cases. The value of the INL for these 100 cases, ranges from 0.7 to 2.7% as shown in the figure. With such response of a DAC, the average degradation of the SNR in a 3-bit second-order $\Sigma\Delta$ modulator (OSR = 32) is 15 dB. Moreover, in power spectral density output, a tone at -79 with $-6\ dB_{FS}$ signal amplitude appears. Using the same mismatch values and the same cases, the proposed technique has been applied considering

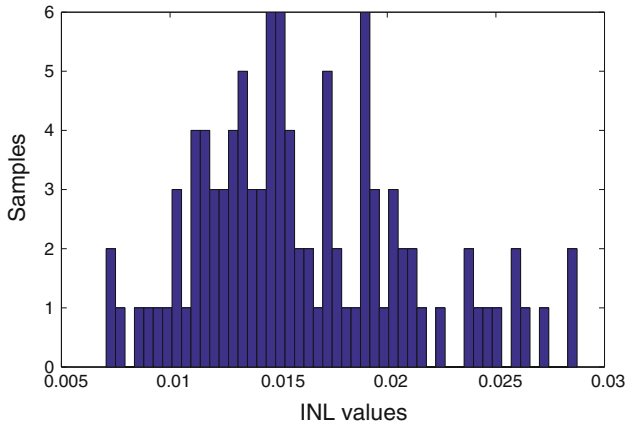

Fig. 5 Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error

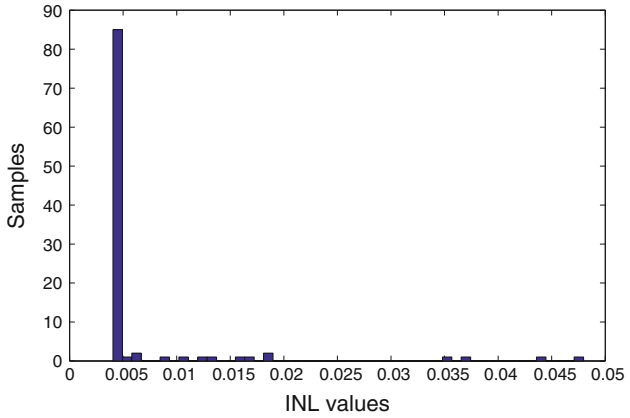

Fig. 6 Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error, after optimum selection

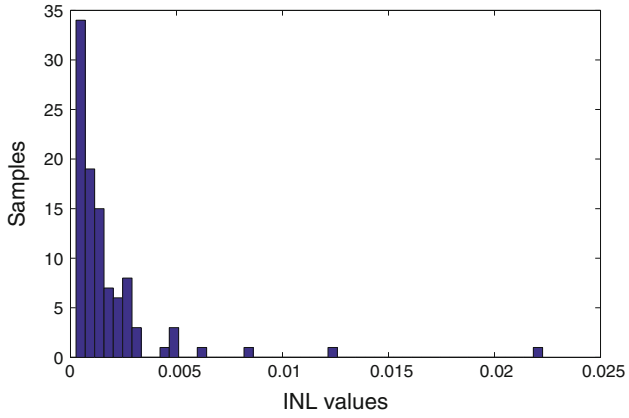

Fig. 7 Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error with optimum selection and nine elements

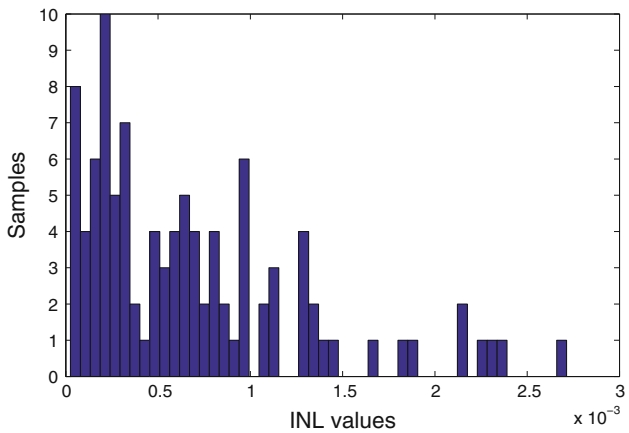

Fig. 8 Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error with optimum selection and 16 elements

only the 8 unity capacitors available for the DAC. The algorithm selects the optimum sequence and obtains the histogram shown in Fig. 6. The capacitors, so the mismatch errors, for both distributions are the same and the only difference is the use of the selection of these capacitors. The distribution that takes advantage of optimum selection is strongly concentrated around 0.005 that it is half the value of the used σ. Moreover, the proper sequence makes the INL plot suitable for smoothing thanks to the random quantization noise variation.

Notice that in order to obtain an INL curve like the one of Fig. 1(b) it is necessary to have pair of capacitors whose value are symmetrical with respect to the average. It means that the distribution of mismatch errors has a mean value of zero. In case of large numbers, this distribution reflects the real case. However, for the case of only eight elements, this may not be the actual case. If, for example, in the set of eight capacitors five elements are bigger and three smaller than the average value, the algorithm cannot pair a bigger and a smaller element. Consequently, the INL will show, somewhere, two consecutive increases.

The histogram of Fig. 6 shows that a small number of cases are not properly brought to a low value of INL. They are caused by the mathematical tails of the statistic distribution that foresee values of unity capacitances with a large error. Indeed, in real situations having a big error is not possible and the real statistical distribution is not with a fully random added term. The result of Fig. 6 denotes a good improvement but some worst cases make the possible yield non acceptable. In order to improve the effectiveness of the method the eight elements are selected from a set with extra elements. The statistic distribution significantly improves even with only one extra capacitor, as shown in Fig. 7. The value of the INL is often below 0.2% with few cases of values larger than 0.6%. The worst situations correspond to the 6–2 distribution around the average because the probability to have 7–1 is almost zero.

Obviously, the use of more element to perform the selection improves the INL histogram. Figure 8 shows that with 16 elements and optimum sequence the INL improves by almost an order of magnitude with respect to the plain case.

Figure 9 shows the INL percentage error respect the ideal case using the algorithm with 8 capacitors, with 16 capacitors and without any calibration for a 3-bit DAC case. Without the algorithm, the INL error is very large, while using the proposed method is strongly reduced and very close to zero. Using more capacitors it is possible to reduce the error and, in particular, it could be reduced for the last code, the one in which are used eight capacitors.

A possible systematic error in the unity capacitor values is transformed into alternate fluctuations of the INL that, as mentioned is smoothed by the effect of the quantization error. Simulation results show that the effect of systematic contributions is negligible until very large gradients that cause an overall change of unity elements as large as 10–15%. In order to show how this technique can be used

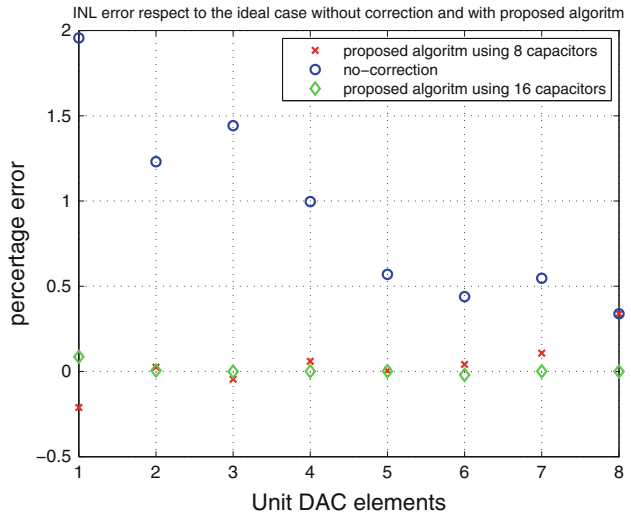

Fig. 9 INL error using the correction algorithm and without

to linearize a multi-bit DAC response, and can improve the ADCs overall performance, many simulations have been performed. As expected, increasing the linearity of the DAC directly improves the ADC response by decreasing the noise floor in the in-band. In Fig. 10(a), proposed method and other methods are compared using a $-3\ dB_{FS}$ input signal: with DEM the SNR is 77.8 dB, while using the proposed method the SNR is 83 dB. The simulation is performed on a second order $\Sigma\Delta$ modulator with 4-bit DAC and OSR = 32. The used mismatch in the DAC elements has a $\sigma = 0.01$.

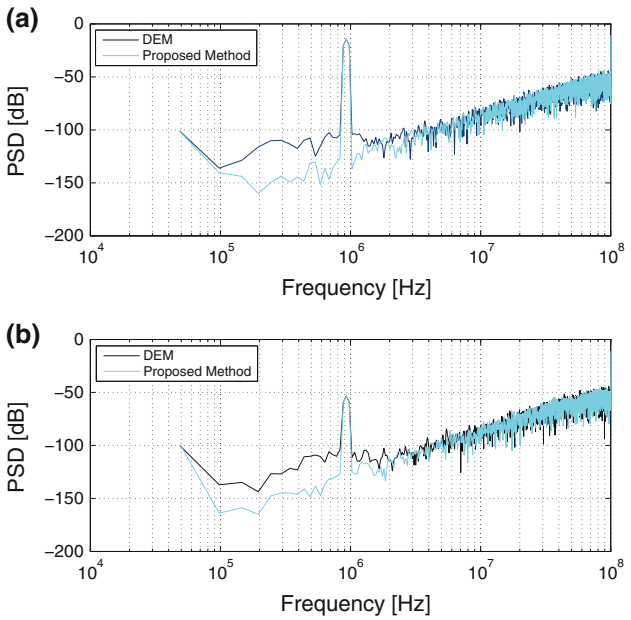

Fig. 10 Output spectra obtained using the proposed method and DWA-DEM with $-3\ dB_{FS}$ input signal (**a**) and with $-30\ dB_{FS}$ input signal (**b**). The capacitor mismatch in the 4-bit DAC is $\sigma = 0.01$

Also, the benefit of the proposed method is not lost for low input amplitude. Figure 10(b) shows that the spectrum obtained with the proposed method still follows the case without mismatch, thus demonstrating the smoothing effect of the quantization noise. A final remark is that with the proposed method the spectrum slope is -40 dB/dec until low frequencies (Fig. 10(a), (b)), while using DEM the noise floor in the signal bandwidth grows. Figure 11 depicts the SNR for the proposed method and DEM changing the signal input amplitude. The capacitor mismatch has a $\sigma = 0.01$. Each dot plotted in Fig. 11 is the average of a 30 runs simulation done on a second order $\Sigma\Delta$ modulator with 4-bit DAC and OSR = 32. The results show better performances at all inputs using the proposed approach.

A preliminary study at transistor level using a CMOS 0.18 µm technology has been performed to estimate the required silicon area, additional power consumption due to calibration, and performances. The comparison covers the results for DEM, the proposed method and the one without any calibration. The simulations are oriented to the design of a second order $\Sigma\Delta$ modulator with 3-bit DAC, OSR of 15, voltage power supply of 1.8 V, and 60 MHz sampling frequency. As mentioned before, the proposed method does not consume any extra-power during the normal operation, whereas in DEM case, there is an increase in power consumption of about 15% respect the case with no calibration. Regarding the area consumption, DEM introduces an area overhead around 25%, while for the proposed method it depends on how many additional unit elements are used in the DAC. Using 8 capacitors the area increases of about 20%, while using 16 elements there is an additional area of about 40%. The results, normalized to the case with no

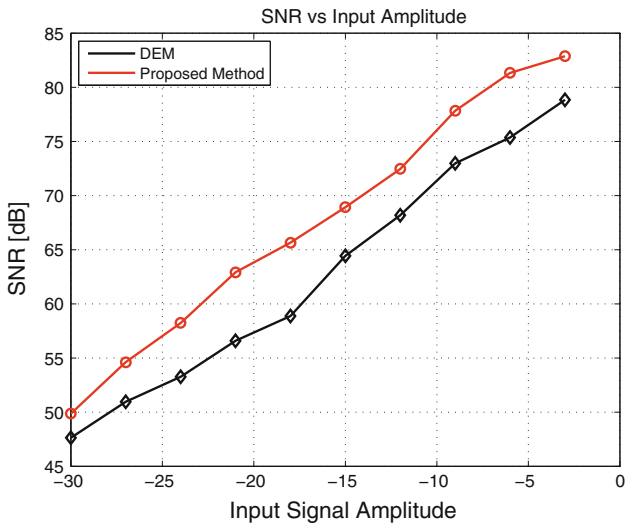

Fig. 11 SNR versus input signal amplitude for the proposed method and DEM. The capacitor mismatch in the 4-bit DAC is $\sigma = 0.01$. Each *dot* plotted in figure is the average of a 30 runs simulation

Table 1 Results of a preliminary study at transistor level to compare the design of a ΣΔ modulator with no correction, DEM, and the proposed solution

	Power consumption	Area	Resolution
No correction	1	1	1
DEM	1.15	1.25	+2-bit
This method using 8 DAC elements	1	1.2	+3-bit
This method using 16 DAC elements	1	1.4	+4-bit

All values are normalized to the case of no correction

calibration, are summarized in Table 1, where the resolution performances are evaluated by behavioral-level simulations.

6 Conclusion

A technique to linearize the multi-bit DAC in ΣΔ-ADC has been proposed. The advantage of the technique is to avoid any run-time power consumption and has the ability to calibrate itself without extra significant hardware overhead. In addition the calibration phase is independent of the oversampling. Any additional unity DAC elements may further improve the performance of the technique so as well the overall system performance without adding any overhead to the power consumption but slightly increase the silicon size depending on how much improvement is needed. Hence the proposed technique has major advantages over DEM and DWA methods especially considering the power consumption.

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structures especially sigma delta ADC's, modelingof analog circuits and compact MOS modeling.

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