Opamp gain compensation technique for continuous-time ΣΔ modulators

V.R. Gonzalez-Diaz, A. Peña-Perez and F. Maloberti

A new method that compensates for the low DC gain of nanometre operational amplifiers (opamps) used for high-speed continuous-time (CT) ΣΔ modulators is described. The proposed solution compensates for the integrator's phase error which is a main limitation produced by the low opamp's gain. The method uses a simple auxiliary gain stage and a resistor. Simulations of a second-order CT ΣΔ modulator utilising fast single-stage opamps with gain as low as 25 dB verify the effectiveness of the method.

Introduction: Very high speed and low power are the key benefits of nanometre technologies. However, scaled processes yield transistors with low transconductance and low output resistance that, in turn, make challenging the design of high-gain opamps [1]. Opamp based integrators are the main blocks of ΣΔ modulators which, for a large signal bandwidth, are normally realised in the continuous-time (CT) form. The use of large bandwidth amplifiers with very low gain causes a shift in the noise transfer function (NTF) zeros, thus causing a drop in the signal-to-quantisation noise ratio (SQNR) [2]. A low DC gain compensation technique [3] can reduce the magnitude and phase errors, but operates in the discrete-time (DT) domain. This method requires an auxiliary switched capacitor structure, but makes the output available only during the injection phase. An alternative method [4] obtains similar benefits, but still works in the DT.

This Letter proposes a new compensation technique which works with CT integrators. It needs little additional hardware and the results show that the required opamp's gain drops from 60 to 25 dB.

CT gain-compensated integrator (CTGC-I): Fig. 1*a* shows a CT integrator, the basic cell of any CT ΣΔ modulator. If the opamp bandwidth is very large (supposed infinite) and the DC gain is low, A_V, the inverting terminal voltage is not zero, but $-V_{OUT}/A_V$, which gives rise to the integrator's response

$$H(s) = \frac{V_{OUT}}{V_{IN}} = -\frac{A_V}{sRC(1+A_V)+A_V} \quad (1)$$

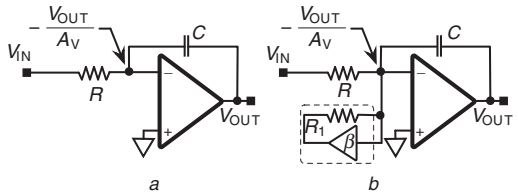

Fig. 1 *CT integrator for analogue*
a Conventional CT integrator
b CTGC-I

Equation (1) denotes a magnitude error equal to $(1+A_V)/A_V$ and a phase error. For $\omega RC = 1$, the phase error is $\arctan[1/(1+A_V)]$. Since the magnitude error changes the integrator's time constant RC, this can be compensated for together with the RC error. The phase error is much more problematic because it damps the integrator and causes a shift of the ΣΔ NTF zeros, inside the z unity circle. The term V_{OUT}/A_V in the resistor, when obtaining the integrator's response (1), causes the phase error whereas the one on the capacitor determines the magnitude error. It is possible to correct the phase error with a suitable current injection into the inverting terminal of the amplifier, as Fig. 1*b* shows. The circuit uses an auxiliary low-gain amplifier (gain is β) to drive an additional resistance R_1, injecting a current into the inverting node. The circuit analysis yields

$$V_{OUT} = -\frac{1}{\left(sRC(1+(1/A_V))+\left(R_1+R-\beta R/R_1 A\right)\right)}V_{IN} \quad (2)$$

The magnitude error is unchanged, but the phase error depends on β and R_1/R therefore on making $\beta = (R_1+R)/R$ the phase error is zero.

The error cancellation can be accurate because the resistor matching is good and a low gain can also be accurate. The gain of the fully differential scheme of Fig. 2, which uses same sizes for the three transistors M_1, M_2 and M_5 and matches M_3, M_4 and M_6, is

$$A_V = \frac{R_2 + 1/g_{m3}}{R_3 + 1/g_{m1}} \quad (3)$$

The gain is R_2/R_3 if $R_2/R_3 = g_{m3}/g_{m1}$. In practical cases, the accuracy is good because in saturation the transconductance of the same type of transistors with equal bias current mainly depends on the aspect ratio.

Behavioural simulations: The gain compensation scheme has been verified in a second-order CT ΣΔ modulator. A verilogA model of the amplifier accounts for bandwidth (supposed large) and gain (assumed low). The sampling frequency is 1 GHz and the oversampling ratio is 48. Therefore, the signal bandwidth is 10.4167 MHz.

Fig. 3 shows the single-ended version of the simulated second-order differential topology. The quantiser is a 3 bits flash ADC and non-return-to-zero DACs. The scheme reduces the output swing of the amplifiers with an analogue feedforward branch ($2R/3$) and the scaling by 2 of the second amplifier output voltage. The doubled capacitance across the second amplifier establishes an equal scaling of the flash references.

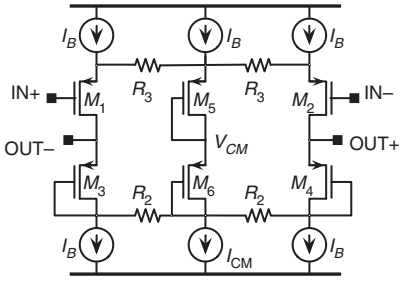

Fig. 2 *Simple amplifier with accurate gain*

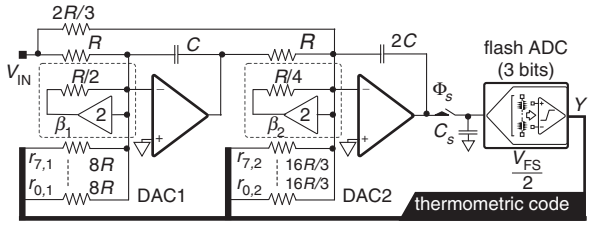

Fig. 3 *Second-order gain-compensated CT ΣΔ modulator*

The behavioural model of the opamps matches the performance of a fully differential single-stage amplifier simulated at the transistor level with a 65 nm technology. The gain is close to 25 dB and the unity gain frequency is 5.2 GHz. The scheme of Fig. 2 shows how the auxiliary amplifiers ΣΔ modulators with $\beta = 2$. The transistor level simulations show that a bias perform current equal to 15% of the current of the main amplifier is enough to ensure a required 5.2 GHz bandwidth. The model supposes a good matching between the resistors of the DACs. The thermometric code generated by the flash controls directly the resistances. If needed, a 3 bit dynamic element matching circuit would transform the error caused by the resistor mismatch into a shaped noise.

Fig. 4 shows the results of simulations. With ideal amplifiers, the SQNR is 89.8 dB. It drops to 52.6 dB with a 25 dB gain on both main amplifiers. As expected, the low gain causes a flat in the noise floor at –70 dB, thus affecting the signal band and degrading seriously the SQNR. It is due to the zeros shift caused by $A_V = 18$ and the 3 bits quantisation

$$\mathrm{NTF}_{z=1} = -40\log_{10}(A_V+1) - 3\times 6.02 \quad (4)$$

With the CT gain compensated integrator (CTGC-I) and the exact cancellation of the phase error the SQNR is 87.4 dB, just 2.4 dB less than the ideal case. That minimum loss is because of the magnitude error, which is not corrected in this simulation. A possible error in the gain of the auxiliary stage, nominally equal to $\beta = 2$, reduces the effectiveness of the phase error cancellation. However, as shown in Fig. 5, the

loss is about 4.3 dB when $\beta_1 = \beta_2 = 2$ change by ± 0.2. Since a low gain factor is realised, for example with the scheme of Fig. 2 is quite precise, the method is robust against the technology variations.

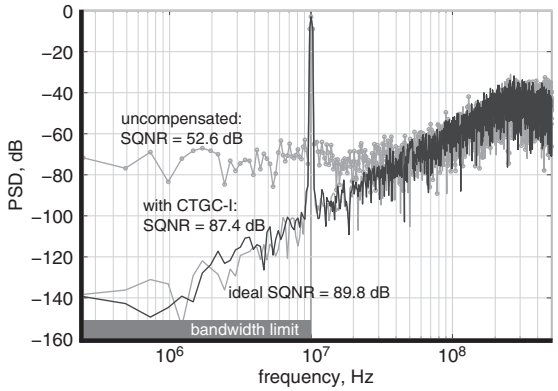

Fig. 4 *Power spectral density comparison, 4096 FFT points*

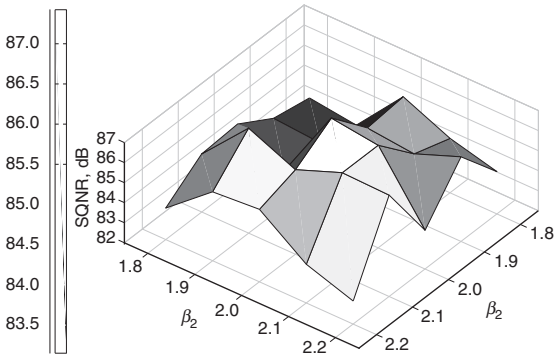

Fig. 5 *SQNR against gain of auxiliary amplifier for first (beta 1) and second (beta 2) integrator*

Conclusion: The proposed compensation scheme of the phase error caused by the low DC gain of amplifiers opens new perspectives for the design of CT ΣΔ modulators running with very high sampling frequency. Simple schemes designed with nanometre technologies achieve unity gain frequencies in the multi-GHz range, but ensuring high DC gain is problematic. This method is a solution to the problem with good robustness against process variations.

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