Opamp gain compensation technique for continuous-time ΣΔ modulators

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A new method that compensates for the low DC gain of nanometre operational amplifiers (opamps) used for high-speed continuous-time (CT) ΣΔ modulators is described. The proposed solution compensates for the integrator’s phase error which is a main limitation produced by the low opamp’s gain. The method uses a simple auxiliary gain stage and a resistor. Simulations of a second-order CT ΣΔ modulator utilising fast single-stage opamps with gain as low as 25 dB verify the effectiveness of the method.

Introduction: Very high speed and low power are the key benefits of nanometre technologies. However, scaled processes yield transistors with low transconductance and low output resistance that, in turn, make challenging the design of high-gain opamps [1]. Opamp based integrators are the main blocks of ΣΔ modulators which, for a large signal bandwidth, are normally realised in the continuous-time (CT) form. The use of large bandwidth amplifiers with very low gain causes a shift in the noise transfer function (NTF) zeros, thus causing a drop in the signal-to-quantisation noise ratio (SQNR) [2]. A low DC gain compensation technique [3] can reduce the magnitude and phase errors, but operates in the discrete-time (DT) domain. This method requires an auxiliary switched capacitor structure, but makes the error cancellation can be accurate because the resistor matching is good and a low gain can also be accurate. The gain of the fully differential scheme of Fig. 2, which uses same sizes for the three transistors $M_1$, $M_2$ and $M_3$ and matches $M_1$, $M_4$ and $M_5$, is

$$A_V = \frac{R_2 + 1/\beta_{\text{in}}}{R_1 + 1/\beta_{\text{in}}}$$

(3)

The gain is $R_3/R_1$ if $R_2=R_3=\beta_{\text{in}}/\beta_{\text{in}}$. In practical cases, the accuracy is good because in saturation the transconductance of the same type of transistors with equal bias current mainly depends on the aspect ratio.

Behavioural simulations: The gain compensation scheme has been verified in a second-order CT ΣΔ modulator. A verilogA model of the amplifier accounts for bandwidth (supposed large) and gain (assumed low). The sampling frequency is 1 GHz and the oversampling ratio is 48. Therefore, the signal bandwidth is 10.4167 MHz.

Fig. 3 shows the single-ended version of the simulated second-order differential topology. The quantiser is a 3 bits flash ADC and non-return-to-zero DACs. The scheme reduces the output swing of the amplifiers with an analogue feedforward branch (2R/3) and the scaling by 2 of the second amplifier output voltage. The doubled capacitance across the second amplifier establishes an equal scaling of the flash references.

$$\text{NTF}_{z=1} = -40 \log_{10}(A_V + 1) - 3 \times 6.02$$

(4)

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loss is about 4.3 dB when $\beta_1 = \beta_2 = 2$ change by $\pm 0.2$. Since a low gain factor is realised, for example with the scheme of Fig. 2 is quite precise, the method is robust against the technology variations.

Conclusion: The proposed compensation scheme of the phase error caused by the low DC gain of amplifiers opens new perspectives for the design of CT $\Sigma\Delta$ modulators running with very high sampling frequency. Simple schemes designed with nanometre technologies achieve unity gain frequencies in the multi-GHz range, but ensuring high DC gain is problematic. This method is a solution to the problem with good robustness against process variations.

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