A 10-bit, 200-kS/s, 250-nA Self-Clocked Coarse-Fine SAR ADC

Yulin Zhang, Edoardo Bonizzoni, Member, IEEE, Franco Maloberti, Life Fellow, IEEE

Abstract—A 10-bit ultra-low power SAR implemented in a standard 0.18-µm CMOS technology is described. The architecture consists of a coarse and a fine SAR ADC. The 2-bit coarse SAR presents the two MSB capacitive arrays of the fine SAR, thus avoiding the largest sources of dynamic power consumption. The use of two low resolution comparators in the coarse converter enables compensating for the offset mismatches between the coarse and fine ADCs. The comparator of the fine SAR obtains high sensitivity and very low power thanks to a gain enhanced dynamic pre-amplifier. A loop delay line generates all the phases for the SAR logic and permits three different modes of operation: on-demand, self-clocked, and clocked. In the clocked mode and 200 kS/s, this converter achieves 9.05 bit ENOB while consuming 200 nW. The resulting FoM is 1.88 fJ/conv.-level.

Index Terms—SAR ADC, ultra-low power, coarse-fine, self-clocked.

I. INTRODUCTION

A NALOG to digital converters (ADCs) are widely used in wireless sensors and healthcare systems, [1]–[4]. Having a power efficient ADC is a key feature to prolong battery life in these applications. A successive approximation register (SAR) ADC can achieve ultra-low power mainly thanks to the simplicity of its structure. In such a converter, the power consumption can be reduced by using an energy efficient capacitive DAC switching method, a low-power voltage comparator, and/or an optimized SAR logic. The power associated to the clock signal for the ADC is always not accounted for. The clock is typically generated outside the chip and brought inside through a pin. However, inputting the clock consumes power that, for ultra-low power ADCs, can be comparable with the one of the converter itself. With 0.8-V supply and input pin-trace capacitance equal to 2 pF, inputting a clock at 200 kHz requires 256 nW, more than what this complete design uses.

In this work, a 2-bit coarse SAR and a fine SAR, made by a 7-bit array plus 2-bit 2C-C stages, work together to reduce the two MSBs fine SAR power consumption. The use of an hybrid DAC structure reduces the number of unity elements of the fine SAR, thus leading to an improved energy efficiency and a smaller area. The pre-amplifier in the voltage comparator includes a cross couple to enhance the gain. A loop delay line generates all the required logic controls, making the logic simpler. The ADC can provide a conversion on-demand or work in the self-clocked or clocked mode. All the digital logic is custom designed to minimize the power consumption. This design is fabricated with a conventional 0.18-µm CMOS technology and operates with a nominal supply voltage of 0.8 V. As a result, the total power consumption is 200 nW. At 200 kS/s and with an input signal close to the Nyquist frequency, the measured ENOB in the clocked mode is 9.05, leading to a FoM of 1.88 fJ/conversion-level.

The paper is organized as follows. Section II describes the ADC architecture and presents the techniques used to achieve ultra low power. The measurement results and the comparison with the state of the art are provided in Section III. The conclusion is drawn in Section IV.

II. PROPOSED SAR ADC ARCHITECTURE

Fig. 1 depicts the fully differential architecture of the coarse-fine ADC. It comprises a 10-bit fine SAR ADC and a 2-bit coarse SAR ADC. The main idea is to relieve the requirements of the fine ADC by a coarse ADC whose accuracy constraint is greatly reduced, [5]. The DAC of the fine SAR is an hybrid structure that combines a binary array and 2C-C stages in order to strongly diminish the total number of unity elements. This brings to both energy and area reduction. The coarse and the fine SARs sample the input at the same time. After the sampling phase, the fine SAR remains in the hold status for the two coarse SAR periods. Indeed, the setting of the first two MSBs (48C_u and three 16C_u) in the fine ADC depends on the coarse SAR ADC outputs. The result enables estimating b7. The double groups of split capacitors are for the b6-b3 estimation; the other capacitors serve for b2-b0.

The coarse SAR ADC consists of two comparators and of a 2-bit DAC, as shown in Fig. 2. The threshold of one of the comparators is shifted up, the other is shifted down of about VR/8 by mismatching the input pairs (VR is the reference voltage). As the coarse SAR is only 2 bit, there is almost no requirement for the resolution of the comparator which can be a simple latch. After sampling, in the first estimation, M, the two latches generate two outputs (d_3, d_2) indicating that the input is well below VR/2, well above VR/2 or in the gray region around VR/2 (see Fig. 2). The second estimation, K, is around 3VR/4 or VR/4 and generates the two other outputs (d_1, d_0). Thanks to the presence of the gray regions, the DAC gain and comparators offset mismatch as the coarse and fine ADCs can be compensated for. The unity capacitor...
used in the coarse SAR ADC is only 3.1 fF and this, together with the use of two simple latches, makes the power of the coarse SAR ADC negligible.

The input signals are sampled onto the coarse and fine ADCs capacitor arrays by means of conventional bootstrapped switches. After the two phases of the coarse SAR conversion, according to the four digital signals $d_3-d_0$ from the coarse SAR, the groups of $48C_u$ and the three $16C_u$ are switched to the reference voltages or to ground for setting one of the levels specified in Fig. 2. The comparator, made by a pre-amplifier and a latch, of the fine SAR decides directly $b_7$ if the DAC setting is at 2/16, 6/16, 10/16 or 14/16 of the full scale. If the setting is in the gray regions, the fine SAR comparator output resolves the uncertainty: if the setting is at half full scale, a logic 1 signifies that $b_3-b_8-b_7$ are 100, while, if the logic output is 0, $b_3-b_8-b_7$ are 011. Similar determinations hold for the two other gray regions. After this, the SAR algorithm continues normally for the remaining bits. The splitting technique, [6], [7], for bits $b_9-b_8$ is the used switching method and the monotonic, [8], for the remaining ones.

Avoiding two cycles in the fine SAR and setting directly the array at the levels of the figure, using two 2C-C sections and the spitting, [6], capacitor technique yield an overall energy reduction of more than 90%. Moreover, since the first setting of the main SAR is close to the input by 1/8 the full scale, the technique moderates possible inaccuracies caused by the common-mode variation of the comparator inputs.

### A. Capacitive DAC

As already mentioned, the capacitive DAC is implemented with a 7-bit binary capacitor array and 2-bit 2C-C structures, [9]. This reduces the number of unity elements of the fine SAR from 1024 to 134 so that the power required to charge/discharge the DAC is reduced by a factor almost 8 with respect to what required by the conventional binary array solution. The DAC only uses 2 bit 2C-C stages because the parasitic capacitances in the floating nodes of the structure degrade the linearity of the DAC array, especially when small unity fringe capacitors are used.

---

**Fig. 1.** ADC block diagram and timing.

**Fig. 2.** Coarse SAR block diagram.

**Fig. 3.** Layout of a unity capacitor.
The DAC of this design uses finger-type metal-oxide-metal (MOM) [10] unity capacitors. The custom layout of a unity capacitor together with the geometrical sizes (compliant with the used technology rules) are shown in Fig. 3. Only top metal layers (M4 and M5) are used in order to reduce parasitics. The resulting unity capacitance is about 3.1 fF, the minimum value allowed by the used technology. The total input sampling capacitance is about 0.4 pF and the total active area is 100 μm x 60 μm.

When using the splitting switching method, [6], after each bit determination, only one capacitor of the DAC array is either switched from ground to the reference voltage (up transition) or from the reference voltage to ground (down transition), as shown in Fig. 4. The energies spent for the up and down transitions are as follows

\[
E_{up} = \frac{V_{ref}^2 C_2 C_3}{C_1 + C_2 + C_3}
\]

(1)

\[
E_{down} = \frac{V_{ref}^2 C_1 C_2}{C_1 + C_2 + C_3}
\]

(2)

To show the effectiveness of the coarse-fine SAR approach of this design, the above equations can be used to calculate the energy spent for determining the first three bits in three cases: a plain 10-bit array driven with the splitting method, an hybrid array with the first 7 bit driven with the splitting method and the remaining with the monotonic one, and the technique used in this design. When the input signal is around half the reference voltage (mid gray zone in Fig. 2), the calculated energies for the first three bits (excluding the initial setting of the capacitive array) are 360 CV\(_{ref}^2\), 22.5 CV\(_{ref}^2\), and 3.5 CV\(_{ref}^2\), respectively.

Fig. 5 shows the calculated switching energy as a function of the output code for three cases: conventional switching algorithm, splitting method, and the technique used in this design. The average switching energies are 1363.3 CV\(_{ref}^2\), 852.3 CV\(_{ref}^2\), and 92.6 CV\(_{ref}^2\), respectively, being V\(_{ref}\) the reference voltage. Compared to the conventional and the splitting methods, this switching algorithm saves 93.2% and 89.1%, respectively.

\[\text{Switching Energy (CV)} \quad \text{Output Code}\]

Fig. 5. Calculated DAC switching energy for three different switching methods: conventional, splitting, and used one.

B. Comparator

Fig. 6 shows the schematic diagram of the fine SAR voltage comparator. The first stage is a voltage amplification stage with V\(_{IN+}\) and V\(_{IN-}\) as differential inputs and O\(_P\) and O\(_N\) as differential outputs. It is a dynamic residual amplifier, [11], in which the use of the cross-coupled pair enhances the gain. Transistors M\(_5\) and M\(_6\) of the pre-amplifier operate as switches when they are on and as (parasitic) capacitive loads when off. The second stage is a conventional regenerative latch that uses two inverters to avoid static current and that achieves rail-to-rail digital outputs, Q and Q\(_N\). C\(_K\) and C\(_{KN}\) are the clocks for the pre-amplifier and the latch, respectively. The pulse width of C\(_{KN}\) is 1.2 times the one of C\(_K\), as shown in Fig. 6.

When C\(_K\)=0 and C\(_{KN}\)=1, the first stage works as an amplifier, while the latch is reset. In this phase, the currents flowing through the input differential pair, M\(_1\) and M\(_2\), charge the parasitic capacitances of M\(_5\) and M\(_6\) (which are switched off) toward V\(_{DD}\). At the beginning, the output voltages O\(_P\) and O\(_N\) increase proportionally to ∆V\(_{IN}\). When the pre-amplifier output voltages, shifted by the threshold of the cross-coupled transistors M\(_3\) and M\(_4\), push M\(_1\) and M\(_2\) in the triode region, because of the cross coupling, one branch weakens, the other becomes stronger, thus increasing the differential gain, as shown by the conceptual waveforms of Fig. 6. When C\(_{KN}\) goes high, the latch starts. Finally, when also C\(_K\) goes high, the parasitic capacitances of M\(_5\) and M\(_6\) are discharged to ground.

Simulation results show that, with a bias current of 2 nA and a differential input signal of 1 mV, the circuit achieves a gain of 12 after 300 ns from the reset. Thanks to the quite large gain
of the pre-amplifier, the sizes of the transistors implementing the latch can be almost minimum, making the circuit power efficient.

C. SAR Logic

Fig. 7 shows the block diagram of the SAR phases generator. A 31-stages delay line generates all the required logic controls. Two inverters, the first one current driven, and a NOR gate make each stage of the delay line. An input signal in the first cell that goes from low to high quickly sets the entire gate make each stage of the delay line. When the input goes low, there is a delay between the input A and the output Y, whose value depends on the current I_B. A simple NOR gate generates the pulse. Four delay cells drive the coarse SAR. Each bit of the fine SAR uses three pulses: one for the pre-amplification phase, one for the latch phase and one for the capacitance array set. The current I_B matches the one of the dynamic pre-amplifier to synchronize speed of the comparator and conversion rate.

As mentioned in the Introduction, the power required for inputting the clock, for ultra-low power ADCs, can be almost the power of the converter itself. To outline costs and benefits, this design can operate in three modes. The logic signals T determine weather the input of the delay line is a pulse for conversions on demand or a clock. Closing in loop the delay line obtains the self-clocked function. For this operation mode, timing accuracy is limited because nA currents controlling an inverter cause non negligible jitters.

Fig. 7 also shows the simple logic that generates the signal C_K for the comparator from the outputs of the delay line. Similarly, C_KV is generated to control the latch. Custom designed D-type flip-flops produce the DAC control signals.

III. Measurement Results

This ADC has been fabricated in a 1P5M 0.18-µm CMOS technology. The chip microphotograph with layout back-annotation and main blocks highlighted is shown in Fig. 8. The ADC core occupies an area of 300 x 350 µm².

Experimental results show that the converter can operate with a supply voltage down to 0.7 V. At the nominal condition, 0.8 V, a bias current in the range 2-10 nA gives rise to a conversion rate ranging in the interval from 50 kS/s to 400 kS/s. Since the jitter of the end of the conversion time is about 2% of it, in the clock-controlled operation mode, the setting of the conversion rate is about 5% lower than the average of the self-clocked value. The overall measured current consumption in the nominal condition and 200-kS/s conversion speed is 250 nA (±2%). The power breakdown is 130 nA for comparator, DAC switching, sampling clock-boosted switches, and 120 nA for the digital part.

Fig. 9 shows the measured output spectrum with a full-scale input signal at 8.05 kHz. The SAR converter is in the self-clocked mode and the sampling frequency is 213 kHz. The achieved SNDR is 59.2 dB, equivalent to 9.55-bit resolution. The SFDR is limited by the second harmonic distortion tone at -63 dBFS. For an input at 8.05 kHz, the limit caused by the jitter is negligible; it becomes evident as the input frequency increases.

Fig. 10 shows the ENOB as a function of the input frequency for two cases: converter working in the self-clocked mode (average clock frequency 215 kHz) and converter synchronized with an external 200-kHz clock. In the self-clocked mode, the jitter mainly causes a resolution drop when the input frequency approaches the Nyquist limit. When an external clock synchronizes, the resolution is about 9 bit for input frequency near Nyquist. Under those conditions, the FoM is
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2016.2538139, IEEE Transactions on Circuits and Systems II: Express Briefs

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART SAR ADCs.

<table>
<thead>
<tr>
<th>Technology [mm]</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
<th>[4]</th>
<th>[5]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage [V]</td>
<td>0.8</td>
<td>0.6</td>
<td>0.6</td>
<td>0.45</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>Sampling Rate [S/s]</td>
<td>80k</td>
<td>16k</td>
<td>100k</td>
<td>100k</td>
<td>200k</td>
<td>200k</td>
</tr>
<tr>
<td>Resolution [Bit]</td>
<td>10</td>
<td>10</td>
<td>11</td>
<td>8</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>ENOB [Bit]</td>
<td>9.1</td>
<td>9.73</td>
<td>10.5</td>
<td>7.5</td>
<td>8.95</td>
<td>9.05</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>200</td>
<td>180</td>
<td>645</td>
<td>120</td>
<td>84</td>
<td>200</td>
</tr>
<tr>
<td>FoM [fJ/conv.-step]</td>
<td>2.4</td>
<td>3.5-20</td>
<td>4.5</td>
<td>6.6</td>
<td>0.85</td>
<td>1.88</td>
</tr>
<tr>
<td>Active Area [mm²]</td>
<td>0.26</td>
<td>0.12</td>
<td>0.03</td>
<td>0.21</td>
<td>0.0065</td>
<td>0.105</td>
</tr>
</tbody>
</table>

REFERENCES


IV. Conclusion

This paper describes design, fabrication and experimental measurements of an ultra low power SAR converter. The obtained results show that with two SARs, one coarse and the other fine, it is possible to optimize the consumed power and limit the swing of the comparator common mode input. The use of 2C-C sections reduces the number of unity capacitors, but parasitics cause non-linearity. For the technology employed in this design, the number of 2C-C cells is 2. The simplicity of schematics allows an operation down to 0.7 V with a conventional 0.18-μm CMOS technology. The fabricated chip achieves, at 200-kS/s and 0.8-V supply, an ENOB of 9.05 bit (Nyquist) and a FoM as low as 1.88 fJ/conv.-level.