Energy-efficient switching method for SAR ADCs with bottom plate sampling

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A high energy-efficiency capacitor switching scheme for successive approximation register (SAR) analogue-to-digital converters (ADCs) is presented. The switching method, verified on a 10-bit SAR scheme that uses bottom plate sampling, achieves an average switching energy and area reduction of 99.32 and 96.5%, respectively, with respect to the conventional solution.

Introduction: Charge redistribution successive-approximation register (SAR) analogue-to-digital converters (ADCs) are nowadays very popular for applications where medium resolution and ultra-low power are the goals. In such a converter, the switching power of the digital-to-analogue converter (DAC), especially for the estimation of the first few bits, is a non-negligible fraction of the total. Recently, several techniques have been exploited to increase the power efficiency of the DAC capacitive array [1–5]. The monotonic switching method [1] achieves 81.2% reduction of the average switching energy (ASE) when compared with the conventional solution. The technique recently reported in [2], an evolution of the so called V_{cm}-based method [3], reduces the ASE by 93.7% whereas the tri-level [4] and the hybrid capacitor [5] schemes achieve remarkable 96.89 and 97.66% ASE reductions, respectively. The above methods use top plate sampling. However, the top plate parasitic capacitors introduce a gain error which can become non-linear if the parasitics are non-linear. In addition, the sampling switch is prone to non-linear clock feedthrough effects that cannot be perfectly compensated for by using clock boosted schemes. Another method to reduce the ASE is described in [6]. The basic idea is to leave floating part of the DAC array during the first cycles of the SAR algorithm. Recent power efficient implementations, based on that method and on an optimisation of the V_{cm}-based technique [7], are reported in [8, 9]. Both solutions, however, use two DAC arrays, one coarse and one fine. Their mismatch may lead to different gain errors. Moreover, the different offset of the two required voltage comparators can cause additional problems. In this Letter, a power and area efficient switching method is presented. It overcomes the above mentioned limits by using bottom plate sampling and a single DAC array. The proposed method, applied on a 10-bit SAR, achieves an ASE and area reduction of 99.32 and 96.5%, respectively, with respect to the conventional scheme.

Proposed ADC structure: The proposed scheme achieves 10-bit resolution while using a single 8-bit DAC array, thus significantly reducing the required power and area. This is possible thanks to a fully differential implementation and to the use of the method reported in [2]. Fig. 1 shows, for the sake of simplicity, the single ended scheme together with the required timing. The DAC is split into a 6-bit (C_u to $32C_u$) and a 2-bit (C_u to $2C_u$) sub-array to further reduce the area. The scheme uses bottom sampling and requires 12 clock cycles for a full conversion.

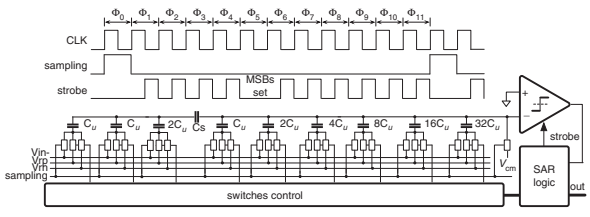

Fig. 1 *Proposed SAR ADC scheme and timing diagram*

Proposed switching method: In conventional implementations, the DAC switching power necessary to determine the first few bits is large because of the large voltage swing and the substantial variation of the top plate voltage. To effectively reduce the consumed power during the first four conversion cycles, this method leaves floating the largest capacitors ($4C_u$ to $32C_u$) and uses the remaining ones to determine the first 4 bits. During Φ_5, the largest capacitors ($4C_u$ to $32C_u$) are set according to the achieved result and the conversion continues following the method described in [2] by still switching only the smallest capacitors of the array.

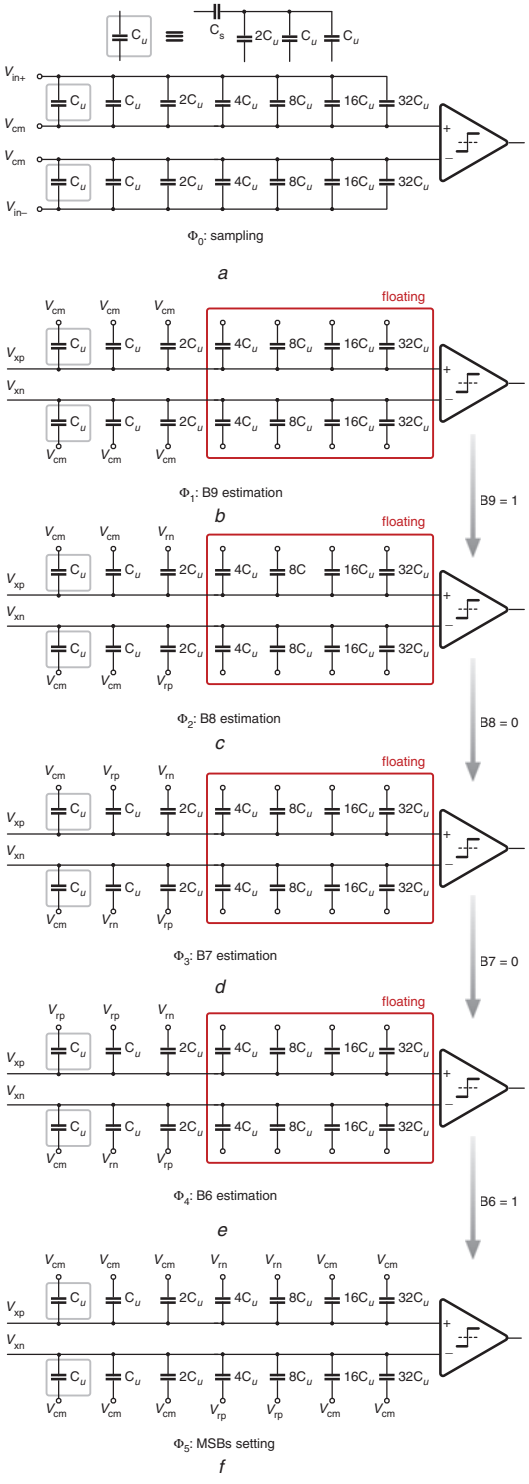

Fig. 2 *Switching sequence example*

Fig. 2 shows an example of the first six conversion cycles. In the figure, the bridge capacitor and the 2-bit sub-array are treated as a unity capacitor. Fig. 2*a* shows the array configuration during sampling: the capacitor top and bottom plates are connected to V_{cm} (half of the reference voltage) and to the input differential signal, respectively. In Fig. 2*b*, $4C_u$, $8C_u$, $16C_u$, and $32C_u$ capacitors are left floating while the remaining ones are connected to V_{cm}. In this condition, the comparator determines B9, the MSB. Supposing that B9 = 1, Fig. 2*c* shows the configuration for the following determination: $2C_u$ capacitors are switched to V_{rp} and V_{rn} (the positive and negative references) while the other capacitors are left unchanged. Fig. 2*d* depicts the configuration for B7 estimation, supposing B8 has been determined equal to 0. For B7 = 0, the configuration of the DAC array for B6 decision is shown

in Fig. 2*e*: note that, for this case, only one of the two smallest capacitors has been switched to V_{rp} while the other remains connected to V_{cm}. Supposing B6 = 1, in this example, B9-B6, the four MSBs, are set to 1001. Fig. 2*f* corresponds to phase Φ_5 of Fig. 1: the information determined by means of the smallest capacitors is transferred to the largest capacitors, which are settled according to the switching method described in [8]. In Fig. 2*f*, the smallest capacitors are reconnected to V_{cm} as a starting point for the remaining decisions. The switching method for the remaining bits continues as described in [2].

An additional benefit of this method is a limited variation of the voltage comparator input common mode. Fig. 3 shows the waveforms at the voltage comparator inputs for the first five phases. It can be noted that the input common mode variation is limited to only one phase (phase 4 in Fig. 3) and is equal to $(V_{rp} - V_{rn})/8$, a value remarkably lower with respect to other methods, [1, 4, 5]. Moreover, thanks to the bottom plate sampling, the possible error is limited to the second order effect caused by the CMRR of the comparator.

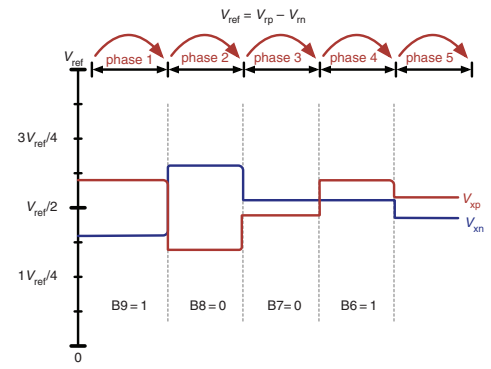

Fig. 3 *Waveforms at voltage comparator input during conversion*

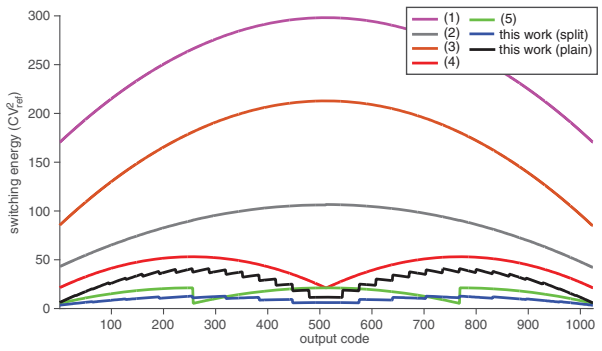

Fig. 4 *Switching energy as a function of converter output code*

Table 1: Comparison of the proposed method with published techniques for 10-bit resolution

Switching method	Average energy (CV^2_{ref})	Energy saving (%)	Area reduction (%)
Conventional	1363.3	0	0
[1]	255.5	81.2	50
[2]	84.9	93.7	75
[3]	170.2	87.54	50
[4]	42.42	96.89	75
[5]	15.88[a]	98.43	75
[9]	229.7	83.15	50
This work (binary)	28.8	97.9	75
This work (split)	9.22	99.32	96.5

[a]$16CV^2_{ref}$ reset energy is not calculated

Switching energy and area estimation of proposed scheme: The behavioural simulation of a 10-bit SAR ADC was performed in MATLAB to compare the proposed method with other recently published techniques. Fig. 4 plots the simulated switching energy as a function of the output code for each method. The method described in this Letter has been applied to two implementations: a 10-bit SAR with split DAC and with binary array. This work achieves 98.9% ASE reduction with respect to the conventional solution when considering a binary array. A further energy reduction is obtained when using the split DAC array: the ASE reduction in this case is 99.3%. Since this method uses a 8-bit array to achieve 10-bit resolution, the area occupation is 75% less than what the conventional solution requires. When using the split DAC array, the area saving is 96.5%. Table 1 summarises the results and provides a comparison with the state of the art. Note that the calculation provided in [5] does not account for an extra $16CV^2_{ref}$ needed during the sampling phase.

Conclusion: This Letter described a power efficient switching method for SAR ADCs. The scheme uses bottom plate instead of top plate sampling to prevent inaccuracies due to parasitic elements non-linearity and sampling switch non-linear clock feedthrough effects. The proposed switching method, while substantially limiting the comparator common mode input range, achieves ASE reduction by leaving floating the largest capacitors in the array during the first conversion cycles. In addition, the technique allows significant area reduction as well. The method, that can be easily extended for any target resolution, has been verified at the behavioural level for a 10-bit SAR. The achieved ASE and area reduction, compared with the conventional solution, are 99.32 and 96.5%, respectively.

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One or more of the Figures in this Letter are available in colour online.

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