High-Resolution Time-Interleaved 8-Channel ADC
for Li-Ion Battery Stack

Dante Gabriel Muratore, Student Member, IEEE, Edoardo Bonizzoni, Member, IEEE, Simone Verri, Franco Maloberti, Life Fellow, IEEE

Abstract—An ADC for monitoring the voltages of a stack of 8 Li-Ion batteries is presented. The converted voltage range for each battery is 3 - 4.2 V with a theoretical maximum input voltage of 33.6 V. High-voltage switches and a single high-voltage capacitor make the high-voltage track & hold. The remaining part of the circuit operates at a nominal 5 V supply. An interleaved extended-range ADC makes the architecture. It converts the 8 channels in 720 μs. The battery monitor has been fabricated in a 0.35-μm triple-well 5V HV CMOS process with drain extended MOS high-voltage devices. The prototype active area is 1300 x 650 μm² and the measured total power consumption is 3.64 mW. The measured input referred noise is 177.9 μV and the residual offset is 642.5 μV.

Keywords—HV switch, Extended Range ADC, Battery Monitor

I. INTRODUCTION

The management of Li-Ion batteries used in electric cars requires the measurement of the voltage across each battery about every 1 ms with an accuracy of 1 mV or better. Since the voltage of a Li-Ion cell can go up to 4.2 V, and several elements are required to achieve high-voltage circuit solutions, this prototype monitors up to 8 batteries, with a relatively simple high-voltage section. The circuit provides a digital conversion of each single cell voltage for a suitable processing of the battery monitor. Existing solutions [1]–[4] employ level shifters and high-voltage control logic for a sequential sampling of the inputs; a SAR or a Σ∆ ADC estimates the outputs. Having multiple high voltage sections grows the silicon area; moreover, sampling the inputs sequentially is not optimal since a common request is made for a sequential sampling of the inputs; a latch with a single stage preamplifier.

This design employs the time-interleaving (TI) of 8 extended range ADCs, [5], [6], made by a 6-bit first order incremental converter and an 8-bit SAR. The track & hold uses only one high-voltage capacitor and 8 high-voltage switches to sample the input, as shown in Fig. 1. The architecture shares the op-amp used in the incremental section and uses a single SAR ADC for all the eight channels. The ADC dynamic range is set accordingly to the Li-Ion battery charge-discharge profile, resulting in a conversion range from 3 to 4.2 V.

This ADC has been fabricated in a 0.35-μm triple-well 5V HV CMOS process with drain extended MOS high-voltage devices. The prototype active area is 1300 x 650 μm². The master clock frequency and the measured total power consumption are 1 MHz and 3.64 mW, respectively. The measured input referred noise is 177.9 μV and the residual offset is 642.5 μV.

II. BATTERY MONITOR

The extended-range conversion of this design foresees two steps. First, a coarse conversion is carried out by an 8-channel time-interleaved first-order incremental ADC. With an oversampling ratio (OSR) equal to 64, the coarse resolution is 6 bit. Each incremental step requires 10 clock cycles (1 for reset, 1 for a dummy channel, and 8 for all the channels), resulting in 640 clock cycles for the coarse stage. Once the first phase is completed, part of the incremental converter is re-arranged as a SAR ADC for the residual voltage conversion. The fine conversion is carried out in 10 clock cycles for each channel, resulting in 80 clock cycles for the whole fine stage. Totally, 720 clock cycles are required for measuring the whole battery stack. Hence, the sampling rate of the overall ADC is equal to 11.1 kS/s (1.39 kS/s each channel), if f_clk = 1 MHz.

In order to achieve the 14-bit resolution required for the entire ADC, the incremental stage uses a two-stage op-amp with large DC gain and suitable bandwidth. Simulation results show that a DC gain of 115 dB and a bandwidth of 20 MHz obtained by a chopper stabilised two-stage amplifier (with a cascode as first stage) match the requirements. The comparator is a dynamic latch with a single stage preamplifier.
A. Coarse step: 8-channel TI incremental ADC

Fig. 2 shows the ADC architecture during the incremental phase. A high-voltage MIM capacitance, \( C_S \), works as a sampling element of all the channels. \( C_{CM} \) provides a shift equal to \( V_{CM,B} = 3.6 \) V, so that a reference voltage of \( \pm 0.6 \) V makes the conversion range from 3 to 4.2 V. Eight nominally equal feedback capacitors, \( C_{ch,i} \), accumulate the charges of the interleaving architecture, and the capacitive bank, \( C_{SAR} \), made by a combined (binary and C-2C) array of unity elements (Fig. 5), operates as an injection element as required by the \( \Sigma \Delta \) incremental function. The left plate of \( C_S \) steps up by one cell at each cycle and injects into the virtual ground, together with \( C_{CM} \) and \( C_{SAR} \), the charge

\[
Q_{\text{inj}} = C_S V_{B,i} - C_{CM} V_{CM,B} + C_{SAR} \frac{V_R}{2} (2D_i - 1)
\]

where \( D_i \) is the output of the comparator at each cycle, \( V_R = 1.2 \) V the reference voltage, and \( V_{B,i} \), the battery cell voltage. \( C_{CM} \) is implemented as a high-voltage capacitor in order to be nominally equal to \( C_S \), and \( C_{SAR} \) is designed to achieve a gain of the incremental stage equal to 1. A possible gain error is compensated for by trimming the value of \( V_R \).

Before each conversion, all the feedback capacitances are discharged. A dummy channel captures the charge injected by the feedback reset switch opening. This avoids a clock feedthrough mismatch on the first battery voltage measurement. Besides, the switch controlled by \( \phi_{CM} \) in Fig. 2 erases any possible memory effect, thus preventing any possible channel cross-talk.

\( C_{P1} \) and \( C_{P2} \) avoid the open loop connection by providing a feedback path to the operational amplifier when no channel capacitor is connected.

Standard solutions call for a low-pass filter in front of the ADC, [1]–[3]. This is usually implemented with external components and results into a filter pole in the range of \([0.1 - 10]\) kHz. In this design, the 64 times sampling of the battery voltage introduces a low-pass FIR filter with 64 taps. This relaxes the performances of the external input filter.

After 64 full cycles, the residual charge stored into each feedback capacitor is

\[
Q_{\text{res,i}} = \sum_{i=1}^{N_{inc}} C_{SAR} \frac{V_R}{2} (2D_i - 1) - N_{inc} (C_{S} V_{B,i} - C_{CM} V_{CM,B})
\]

where \( N_{inc} = 64 \) is the number of incremental cycles.

Since the signal is accumulated 64 times and the noise is quadratically superposed 64 times, the incremental phase attenuates the \( kT/C \) noise request by \( \sqrt{64} = 8 \).

The use of a chopper-stabilised op-amp significantly reduces the input referred offset. The residual offset is mainly due to the charge injection mismatch caused by the opening of the switches connected to the virtual ground. A careful design and layout of the op-amp keeps the error below 0.5 LSB and no calibration is required.

B. Fine step: SAR ADC

The 64 x 8 incremental cycles achieve a 6-bit resolution for each channel. The \( C_{ch,i} \) capacitors store the residual charges. For extending the range, the architecture is re-arranged as in Fig. 3. Fig. 4 shows the transfer of the residual voltage from the \( C_{ch,i} \) capacitors to \( C_{SAR} \). The chopper operation is disabled and the \( C_{SAR} \) array is pre-charged to the offset of the op-amp in an auto-zero fashion (Fig. 4(a)). Then, the residual charges...
are sequentially transferred to $C_{SAR}$ in order to perform the SAR conversion cycles (Fig. 4(b)).

The relaxed accuracy constraints of the second conversion stage allow to use a DAC array, $C_{SAR}$, made by a combined 5b-binary and 3b-C-2C structure (Fig. 5). The array is composed by 41 poly capacitors $C_U$ of 40 fF. The total capacitance results in $C_{TOT} = 1.64$ pF. The SAR uses the same comparator of the incremental converter and recycles the 1-b DAC to control the bottom plates of the capacitances.

Since both incremental and SAR steps use $C_{SAR}$ for balancing the input, there is no mismatch between the two phases. Moreover, input sampling and voltage shift use the same type of high-voltage capacitors. A minor limit can come from the mismatch among feedback channel capacitors, $C_{ch,i}$. Their role is to generate the voltage driving the comparator during the incremental phase. Since the mismatch changes the amplitude but not the sign, the possible error is in the dynamic output of the op-amp. It is just necessary to keep the operation in the linear region for avoiding harmonic distortion.

III. HIGH VOLTAGE TRACK & HOLD

Fig. 6(a) shows the scheme commonly used for a bi-directional high-voltage switch driven by a low-voltage logic control. A back-to-back pMOS configuration with extended drain avoids diode forward biasing when the biasing of the switch reverses. In order to turn on the transistors, a low-voltage clock signal, CLK, is used. When the clock signal is high, the current $I_{SW}$ through the resistor $R_{SW}$ generates the proper $V_{sg}$. A high-voltage nMOS transistor, tied to

$V_{DD, LV} = 5$ V, ensures that the drain node of the low-voltage transistor does not exceed $V_{DD, LV} - V_{th}$. This solution is suitable for low accuracy or logic signals. For precise applications, the current $I_{SW}$ flowing in $R_{SW}$, used to turn on the transistors, also flows through one of the two back-to-back p-channel elements and this causes a non-linear drop $△V$ that generates an offset affecting the sampled voltage, Fig. 6(b).

The value of $V_{sg}$ chosen to give rise to the on-condition is the $R_{SW} I_{SW}$ product. The choice of the $V_{sg}$, the $R_{SW}$ value and the required speed of operation determine the minimum (non-linear) $r_{on}$. Indeed, there is a maximum size for the transistors, since their gate capacitance and the value of $R_{SW}$ give rise to a limiting time constant. It is possible to reduce the time constant with lower values of $R_{SW}$ but $I_{SW}$ increases and augments the generated offset. The result is that the speed of operation critically affects the on-resistance of the switch. Extensive simulations at the transistor level show that the offset (the product of $I_{SW}$ and the on-resistance) is, for a sampling frequency of 1 MS/s, much larger than the expected LSB. This circuit solves the problem by using a matched dummy structure that generates the proper $V_{sg}$. The control voltage is then used to drive the actual switch, as shown in Fig. 7. In this way, no static current flows through the sampling switch and the required accuracy is achieved. The non-linearity of the on-resistance is ineffective if the sampling period is a suitable number of time constants $r_{on} C_S$.

This design uses an optimal power, speed and silicon area trade-off that leads to $I_{SW} = 80$ µA, $R_{SW} = 50$ kΩ and

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**Fig. 4.** Mismatch cancellation technique during charge transfer to $C_{SAR}$. (a) Auto-zero phase. (b) Charge transfer from incremental channel to SAR array.

**Fig. 5.** $C_{SAR}$ array architecture. 5 bits are implemented in a binary fashion, and 3 bits use a C-2C structure.

**Fig. 6.** High-voltage track & hold. (a) Schematic. (b) Offset due to $r_{on}$.

**Fig. 7.** Proposed high-voltage track & hold with dummy structure.
The simple structure of the switch results in an area-per-switch of 0.006 mm², significantly smaller than the solutions in [8], [9]. Moreover, the circuit implementation does not require high-voltage capacitors to operate.

IV. MEASUREMENT RESULTS

This ADC has been fabricated in a 0.35-μm triple-well 5V HV CMOS process with drain extended MOS high-voltage devices. The prototype has been measured with the nominal supply voltage of 5 V and its active area is 1300 x 650 μm².

Fig. 9 depicts the whole chip microphotograph and a magnified view of the active area, where the main circuitual blocks have been highlighted. The large area occupied by the high-voltage front-end is due to comply with the minimum ESD distance rules of the used technology. The low voltage section mass formed by the op-amp, the comparator and the capacitors bank (8 channels, 1 dummy channel, 1 SAR/feedback bank). The capacitor injecting the battery common-mode, \( C_{CM} \), and \( C_S \) are both high-voltage with a well matched layout in the HV section. Finally, the low-voltage digital logic provides all the control signals to the system.

Fig. 10 shows the histogram of 300 repeated measurements on channel 1, with the input shorted to \( V_{CM} \), which is at half scale of the converter. It measures the input referred noise, whose variance is 177.9 μV, and the residual offset, equal to 642.5 μV.

Fig. 11 gives the measured output spectrum with a full scale sine wave (0.6 V peak value) at 2.78 Hz applied on channel 8. The SNDR is 76.7 dB (12.45 bit). The harmonic tones amplitude is very low and limits the SFDR at -96 dBFS.

Fig. 12 shows the measured INL resulting from the histogram of a full scale input sine wave on channel 4. The INL is in the [-2,0.5] LSB range. Similar both static and dynamic results have been collected from all the channels. The endpoint fit line INL shows a good linearity of the high-voltage capacitor \( C_S \) in the ±0.6-V range. The linearity over the full 33.6-V range depends on the voltage coefficients of the high-voltage capacitor, \( C_S(V) = C_S(0)(1 + \alpha V) \). Fig. 13 shows the nonlinearity error of the measured outputs (average of 100 measurements) when the same input is applied to all the channels (\( V_{Bi} = 3.6 \) V). The result is the difference with respect to the first channel output and is expressed in LSBs.
The error is almost the same for all the available chips and can be corrected in the digital domain.

The achieved accuracy at room temperature over the whole dynamic range, after channel calibration according to Fig. 13, is about ±1 mV.

Fig. 14 shows the system power breakdown with 1 MHz master clock frequency. The total power consumption is dominated by the digital logic and is equal to 3.64 mW.

Table I summarises the battery monitor performances and provides a comparison with existing solutions. The comparison is performed by using the Schreier figure of merit, $F_{OM} = \text{SNR} + 10 \log(BW/\Delta f)$, [10]. In this design the SNR, the bandwidth and the power consumption are 76.7 dB, 700 Hz and 3.64 mW, respectively. The resulting $F_{OM}$ is 129.5 dB. The achieved results are competitive, considering that the works reported in [1] and [3] can measure only up to 6 cells. The system in [4] implements a parallel solution that uses 6 transimpedance amplifiers (TA) as level shifters, and 6 $\Sigma\Delta$ ADCs. This overhead in complexity is likely paid in larger power consumption and occupied area. Besides, the inter-channel matching becomes a major concern in parallel architectures.

V. CONCLUSIONS

In this paper, a battery monitor system was presented. The architecture uses a time-interleaved incremental converter for coarse conversion and a single SAR ADC for fine conversion. A HV track & hold with low-voltage logic control interfaces the A/D with the battery stack. This solution achieves high linearity and low cost.

The battery monitor has a resolution of about 0.2 mV, consuming 3.64 mW with an area of 1300 x 650 $\mu$m$^2$. All channels are measured in 720 $\mu$s. The measured residual offset is 642.5 $\mu$V.

REFERENCES