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Reprinted from
IEEE JOURNAL OF SOLID-STATE CIRCUITS
Vol. 23, No. 6, December 1988
A Tunable Switched-Capacitor Programmable N-Path Tone Receiver and Generator

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Abstract — An integrated full-duplex tone receiver and generator used for signaling in mobile radio systems and realized with a switched-capacitor pseudo N-path technique is described. A receiver filter with a quality factor programmable in the range 10–230 with an in-band loss less than 0.2 dB and center frequencies from 1 Hz up to 10 kHz was achieved. The tone generator of the system was realized with a programmable gain switched-capacitor (SC) amplifier that generates an eight-sample pseudosine-wave signal. The chip was fabricated using a 3-μm double-poly CMOS process. Its power consumption is 17 mW with a single 5-V supply and its size is 18 mm².

1. Introduction

Modern communications systems make use of tones in the audio and/or subaudio frequency band for signaling functions. In usual applications, as for example in DTMF signaling, a small number of different frequencies are selected. However, there exist other cases, such as mobile radio systems, where the tone frequencies may be different from one application to another. In these cases, receivers and transmitters which are widely programmable in their parameters are useful because they can be tailored to the tone standards of a specific application. An important feature of a tone receiver is the selectivity. It is determined by a trade-off between the minimum transmitted signal power, the internally generated noise, and the maximum allowed detection time. In fact, a high selectivity increases the signal-to-channel-noise ratio at the output of the filter, but implies at the same time longer detection times and higher receiver noise. An optimum quality factor value $Q$ for specific mobile radio systems can range typically from 10 to 200. The selectivity requirements are satisfied using an $N$-path filtering structure, since it is able to guarantee high $Q$ values with relatively low sensitivity to component variations [1]–[3].

As far as the tone generator is concerned, the tones must be programmed at the same frequencies as the receiver center frequencies, and be as free as possible from high harmonic components.

In this paper an integrated CMOS circuit which implements in a single chip a tone receiver/generator for mobile radio systems is described [4]. The resonant frequency, the $Q$ of the receiver filter, and the tone frequency of the generator are all digitally programmable. The analog parts of the system are realized with sampled-data switched-capacitor (SC) circuits.

II. System Description

A block diagram of the overall system is shown in Fig. 1. It contains two different sections: one for the analog signal processing, the other for the digital control and the interfacing. In the analog section, the signal is applied to a sampled-data bandpass filter which is realized with a pseudo N-path SC structure. The N-path configuration was employed since it gives some important advantages over other active approaches [1], [2].

The notch filter cascaded with the N-path filter cancels the passbands at dc and at even multiple integers of the fundamental frequency $f_s/N$, which are introduced by the pseudo N-path operation.

The tone detection is accomplished by the tone detector block of Fig. 1 which is formed by a full-wave rectifier cascaded with a low-pass filter and a Schmitt trigger.

The transmitted tone is generated within a block which employs the same clock phases as those used for the receiver filter. It synthesizes a sampled pseudo-sine-wave signal with $N$ samples per period.

The digital section contains two programmable counters, a clock phase generator, and a 17-bit shift register. The first 12 bits stored in the shift register control the two counters and establish the center frequency of the receiver filter. The other 5 bits are used to program the $Q$ of the N-path filter. The blocks of the scheme in Fig. 1 are described in more detail in the following sections.

Manuscript received November 9, 1987; revised May 30, 1988.
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IEEE Log Number 8824166.
Fig. 1. Overall system schematic block diagram.

Fig. 2. SC damped integrator.

Fig. 3. SC pseudo N-path filter. (a) Schematic block diagram. (b) Clock phases.
A. The Pseudo N-Path SC Filter

The basic cell for the pseudo N-path SC filter is the simple first-order damped integrator shown in Fig. 2. Its z-domain transfer function is given by

\[ H(z) = \frac{C_1 / C_3}{1 + C_2 / C_3} \]  \hspace{1cm} (1)

The N-path filter transfer function can be obtained from (1) simply by replacing the complex variable \( z \) with \( z^N \), where \( N \) is the number of storage elements. In order to guarantee that the residual ripple of the rectified signal will be lower than the hysteresis of the Schmitt trigger, the number \( N \) of parallel paths is set equal to eight. Hence the actual N-path z-transfer function is given by the following equation:

\[ H(z) = \frac{C_1 / C_3}{z^8(1 + C_2 / C_3) - 1} \]  \hspace{1cm} (2)

This transfer function for \( z = \exp(j\Omega T_s) \) shows a comb frequency response with passbands at \( f = f_s / 8 \) (i = 0, 1, 2, \ldots) and bandwidth \( BW = BW_p / 8 \) (\( BW_p \) is the original damped integrator -3-dB bandwidth). Equation (2) shows that, at any instant \( nT_s \), the output is obtained by integrating the last input sample with the charge that has been stored eight sampling intervals before.

There are different pseudo N-path SC cells that are suitable for implementing (2) [1]. They differ in the manner through which the \( N \) time-slot delay is generated for each of the \( N \) integrations. The cell chosen here is the SC RAM-type cell and the resulting pseudo N-path SC filter is shown in Fig. 3(a). \( C_1 \) is the integrating capacitor, \( C_1 \) and \( C_2 \) are the input and the damping capacitors, respectively. Both of them are formed by an array of appropriate capacitors to be used for \( Q \) programming while keeping the in-band gain at 0 dB. Capacitors \( C_4, C_5, \ldots, C_H \) form the analog RAM array for the N-path operation. Fig. 3(b) shows the clock phases used to control the status of the switches. The filter operation is briefly described as follows: when phase \( \phi_1 \) is on, the capacitor \( C_4 \) is active in the analog RAM array. During phase \( \phi_2 \) the charge stored in \( C_4 \) (eight time intervals before) and the input charge on \( C_1 \) are both transferred through the virtual ground and summed on the parallel capacitance \( C_2 + C_3 \). During \( \phi_3 = 1 \) the newly updated charge on \( C_1 \) is injected back on \( C_4 \) where it is stored for the next seven time intervals, until phase \( \phi_4 \) rises again. At the same time, \( C_1 \) is charged by a new input sample and \( C_2 \) is discharged to ground. The same operation cycle is then repeated during each of the other subintervals \( \phi_2, \phi_3, \ldots, \phi_8 \). The phase \( \phi_{res} \) is used to discharge rapidly the receiver filter when initialization of the system is required.

B. The Notch Filter

As mentioned above, the frequency response of the pseudo N-path SC filter is a periodic function and its period is equal to one-eighth of the sampling frequency \( f_s \). Because of this, the tone signaling frequency range would be inconveniently limited since the second passband may lie in the operating frequency range. In order to solve this problem, a fourth-order programmable bandpass prefilter with center frequency at the fundamental resonant fre-
Fig. 6. SC tone generator. (a) Schematic diagram. (b) Clock phases.

Fig. 7. Digital section schematic block diagram.

frequency would be needed; this prefilter, however, is very expensive. An alternative and more efficient solution to increase the signaling tone range while reducing the prefilter complexity is to employ the N-path FIR filter shown in Fig. 4(a). Its z-transfer function is

$$H(z) = \frac{C_1}{C_2} (1 - z^{-4}).$$

(3)

In this filter the frequency response is zero at \( f_s = 2df_s/8 \) \((i = 0, 1, 2, \ldots)\). The filter operation is based on the same analog RAM concept as used for the pseudo N-path filter. The capacitors \( C_1, C_2, C_3, \) and \( C_4 \) (nominal equal to \( C_1 \)) hold a storage charge proportional to the signal which was present one, two, three, and four time intervals before, respectively. When phase \( \phi_4 \) is on, the capacitor \( C_4 \) is the active element. During phase \( \phi_4 \) its charge and that coming from the input capacitor \( C_1 \) are injected into the virtual ground with opposite polarity. The difference between the two charges is stored on the capacitor \( C_1 \) (with \( C_1 = 2C_1 - C \)) and it defines the current output sample as \( V_{out}(nT) - V_{out}(nT-4T) \). Next, when \( \phi_4 \) is on, the capacitor \( C_2 \) is discharged to ground while \( C_1 \) transfers its charge onto \( C_4 \). This operation is repeated during the other phases \( \phi_2, \phi_3, \) and \( \phi_4 \).

C. The Tone Detector

The last block in the receiver section is the tone detector shown in Fig. 5. It is formed by a low-pass filtered full-wave rectifier cascaded with a time-continuous Schmitt trigger. The filtering and rectifying operations are actually performed by the same damped integrator, where the input structure is switched to inverting or noninverting configuration according to the sign of the incoming signal. To avoid undesired dc coupling effects with previous stages, Inoue and Ueno’s integrator was employed [5]. Here a parasitic-compensated input structure is used to get, depending on phase \( \phi_s \), either positive or negative SC toggle operation. Phase \( \phi_s \) is controlled by the input signal sign. In order to keep the residual ripple of the filtered and rectified signal below the trigger hysteresis, a large time constant and hence a large capacitance spread \( (C_1/C_2) \) was necessary for the low-pass filter. Although techniques to obtain very large time constants with relatively small capacitance spread are available [6], the leakage error they introduce at low sampling frequencies did not allow their use in our application. The Schmitt trigger is simply a comparator with hysteresis; the positive feedback around it was realized with p-well diffused resistors.

D. The Tone Generator

The tone generator produces an eight-sample pseudo-sine-wave signal inherently at the same frequency as the one to which the receiver is tuned. Sine-wave signals are generally obtained with periodic square waves [7] or SC oscillators followed by smoothing filters [8], [9]. Another way to realize a sine-wave signal is to use digitally gain-controlled amplifiers. In our case, the availability of the
eight clock phases generated for the N-path filter suggests the simple solution shown in Fig. 6(a), which employs an offset-insensitive SC amplifier. In this circuit, the capacitors \( C_1 \) and \( C_2 \) are equal to \( \sqrt{2}/2 \cdot C \) and \( (1 - \sqrt{2}/2) \cdot C \), respectively, while \( C_3 \) is equal to \( C \). During time slot "1," \( \phi_1, \phi_2, \) and \( \phi_3 \) are activated; hence the op-amp is in buffer configuration, \( C_1 \) and \( C_2 \) are charged to the difference between the op-amp offset voltage \( V_m \) and a reference voltage \( V_{ref} \), and \( C_3 \) is charged to \( V_{ref} \). During time slot "2," \( C_3 \) acts as a feedback capacitor and \( C_1 \) injects its charge into the virtual ground. Therefore, the first nonzero output sample takes the value \( \sqrt{2}/2 \cdot V_{ref} \). By following the other time slots in the scheme shown in Fig. 6(b), it is possible to see that they generate eight values of a pseudorandom signal of \( V_{ref} \) amplitude.

E. The Digital Section

The digital section can be divided in three blocks: a frequency scaler, a clock phase generator, and a serial-to-parallel interface register (Fig. 7). The frequency scaler is made by two programmable synchronous binary counters, with three and nine stages. The three-stage counter carries a prescaler operation for the nine-stage counter; both counters are utilized when the tone receiver/generator operates in the subaudible frequency range, while only the nine-stage counter is activated if the tones are generated in the audio frequency band. The nine-stage counter alone divides the master clock by a factor selected in the range 4–511. The clock phase generator controls the analog circuit switches; it is a sequential synchronous network, composed of two-four-stage Johnson counters and driven by the main clock frequency \( f \).

The last block realizes the interfacing with the external system and programs the tone receiver/generator parameters. In order to reduce the number of the pins and hence the external connections to the chip, serial programming was employed at the expense of a more complicated microprocessor software.

The programming binary word is composed of 17 bits; five of these establish the N-path filter \( Q \) values, and the other 12 define the ratio factor of the counters. These bits are serially charged into two parallel shift registers, of nine and eight stages. Next, they are transferred into 17 latch stages, which are controlled by two strobe signals. This loading procedure makes the microprocessor operation easier since only the eight less significant bits, which determine the receiver/generator tone frequency, are usually changed.

III. Design Considerations

The analog building blocks (op amps, comparators, and the Schmitt trigger) were designed using the SPICE simulator [10]. The op amp used throughout the system is a typical two-stage transconductance scheme with Miller pole-splitting compensation. Its electrical performances are summarized in Table I. A similar scheme was used for the comparator in the Schmitt trigger. Here, however, the branch currents and the transistor geometries were appropriately modified and the compensation capacitor was removed to optimize the circuit for its open-loop operation. In order to have an estimate of the SC circuit settling times, SPICE simulations were carried out on the simple integrating structure described in Fig. 2, where a real op amp and real switches were introduced. The results of these analyses were extended to design the SC analog stages actually used in the system. The overall circuit was simulated in both the time and frequency domains with a SWITCAP simulator [11]. It was also possible to evaluate typical parasitic effects in the SC circuits.

In our system, a critical error source was found to be the leakage currents, since the system has to be operated at very low sampling frequencies. Measurements made in the range 5–15 V show a quasi-linear dependence of these currents on the junction voltage [12]. This allowed the modeling of the leakage effects by means of a grounded toggle capacitor switched from a dc voltage generator to the leakage node. The digital section was designed using a standard cell semi-custom approach and the layout was obtained using the AMI SCOPRE II [13] system on a personal computer. The timing verification and the fault analysis were performed by the TEGAS simulator [14].

IV. Experimental Results

Experimental measurements were carried out on several integrated samples. The frequency response of the pseudo N-path filter cascaded with the FIR notch filter, for different...
Fig. 9 Measured frequency response of pseudo N-path with notch filter for different clock frequencies ($Q = 20$).

Fig. 10 Zero-input signal noise measured pattern at the pseudo N-path filter output (resonant frequency = 8 kHz, $Q = 76$).

Fig. 11 Pseudo N-path: measured zero-input signal noise versus $Q$ values.

Fig. 12 Tone-generator measured output spectrum.

Fig. 13 (a) Pseudo N-path filter output signal, $f_0 = 8$ Hz (b) Tone-generator output signal, $f_0 = 8$ Hz.

Fig. 14 Chip microphotograph.

ent $Q$ values, is shown in Fig. 8. As can be seen, the center frequency attenuation is less than 0.2 dB, for $Q$ values from 10 to 230.

The frequency responses for different clock frequencies and $Q = 20$ are illustrated in Fig. 9. These curves show the notches at $f_i = 2f_0/i$ ($i = 0, 1, 2, \ldots$). At these frequencies the attenuation is greater than 40 dB. Fig. 10 shows the time-domain zero-input signal noise pattern at the N-path filter output. This noise is caused principally by the charge injection which is due to the clock feedthrough; its dependence on the $Q$ value is approximately linear, as shown in Fig. 11. Since the op-amp output swing is about 4 $V_{pp}$, the dynamic range of the N-path filter is better than 40 dB for $Q$ values less than 100.
The tone generator output spectrum is shown in Fig. 12. The harmonic attenuation within the Nyquist frequency range is more than 50 dB. The folding of the harmonic components over the Nyquist range does not give any problem in the receiver section, since they are cut by filters of the external system.

One more notable characteristic of the chip is its performance at very low sampling frequencies. Measurements at 80°C have shown a correct behavior of the receiver filter and the tone generator, with good immunity to leakage currents, at sampling frequencies less than 10 Hz. Fig. 13(a) and (b) shows the receiver-filter and the tone-generator measured output signals at 1 Hz ($f_s = 8$ Hz), respectively.

A microphotograph of the chip is shown in Fig. 14.

V. CONCLUSIONS

An integrated CMOS full-duplex tone receiver/generator for a mobile radio system with programmable center frequencies and $Q$ values has been described. The flexibility of the chip allows its use as a general-purpose tone receiver and generator for a wide variety of signaling standards.

The tone receiver uses an eight-path pseudo-$N$-path filter cascaded with an $N$-path FIR notch filter and a detection circuit. The tone generator produces an eight-sample pseudo-sine-wave voltage at the same frequency as that of the tone-receiver center frequency. The chip has been integrated in a 3-μm double-poly CMOS process; its area is 18 mm². The design was carried out jointly by Italcell and the Electronics Department of the University of Pavia. The chip was built by AMS (Austria Mikro Systeme International).

Experimental results have confirmed the effectiveness of the pseudo-$N$-path SC filter technique in tone receiver/generator applications with operating frequencies as low as 10 Hz.

REFERENCES


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From 1983 to 1987 he worked there, on scholarship, in the Faculty of Engineering. He has actively contributed to the development of an integrated mobile radio design in collaboration with Italnet and AMS (Austria Mikro Systeme). Since 1987 he has been employed at the Department of Electronics of the University of Pavia, where he has been doing research in the field of analog integrated CMOS circuits. His main research interests include, particularly, operational amplifiers, power amplifiers, and switched-capacitor circuits.