Far-field measurements were made on a different 10 × 7 (seven gain sections) array from the same wafer. At power levels near 1 W, the FWHP of the longitudinal far-field was 0.04° (similar to Fig. 5 of Reference 4) and increased to 0.65° at 7 W.

Acknowledgments: The authors would like to thank W. Reichert and J. Kirk for much of the device fabrication work, R. Farkas for device mounting, S. K. Liu for probe testing, J. Hunt for Faber development and J. M. Hammer, S. L. Polfre, R. Amantea, R. Bartolini, and M. Ettenger for technical discussions. This work was supported in part by the Department of the Air Force.

G. A. EVANS 15th June 1990
N. W. CARLSON
D. P. BOUR
M. LURIE
David Saroff Research Centre
CN 5200
Princeton, NJ 08543-5300, USA
R. K. DEFREEZE
D. J. BOSSERT
Department of Applied Physics and Electrical Engineering
Oregon Graduate Centre
19500 N. W. Y. Von Neumann Dr.
Beaverton, OR 97009-1999, USA

References
5 PHILLIPS, R. H. 'Microchannel heat sinks', The Lincoln Laboratory Journal, 1988, 1, (1), pp. 31–48

AUTOMATIC SWITCHING OF SUBSTRATE BIAS OR WELL BIAS IN CMOS-ICs

Indexing terms: Integrated circuits, Comparators (circuits), Metal–oxide–semiconductor structures and devices

A circuit for automatic bias voltage switching in CMOS-ICs is presented. It allows the chip substrate (or the well) to be biased at the highest (or lowest) voltage, even when the input exceeds the supply. Experimental measurements on integrated samples are shown.

Introduction: In many applications the voltage at the input of a CMOS-IC may exceed the positive or negative biasing of the circuit. When the input terminal is connected to the source or to the drain of an MOS transistor, even for protection purposes, a direct bias of the source (or drain)–substrate (or well) diode may occur. If the input source has low impedance, a large power is dissipated and damage to the circuit is possible. In such situations it is necessary to control the biasing of the chip substrate or to control the biasing of the well in which the transistors connected to the input terminal are placed. With a p-well technology and p-channel input tran-
sitors, input signals above $V_{dd}$ are dangerous. Conversely, if the input transistor is an n-channel device, input voltages below $V_{ss}$ cause problems. Complementary situations occur for an n-well technology. These problems can be resolved by automatic switching of the substrate bias (or the well bias) between the supply and the input voltage.

A comparator designed to perform this function is described here.

Circuit description: The circuit was designed for the correct biasing of the substrate in a CMOS p-well technology; it can also be used for the well biasing in an n-well technology. A complementary circuit can be used for switching between $V_{dd}$ and $V_{ss}$.

The circuit shown in Fig. 1 is a differential stage with two symmetrical parts directly powered by the input terminal and by $V_{dd}$ respectively. Apart from the unconventional separate powering of the two symmetrical sections, the circuit made up of M1–M8 is a single stage mirrored amplifier, whose inputs are the voltages $V_{in1}$ and $V_{in2}$ shifted down by $V_{LSB}$. The purpose of the separate biasing is twofold: increasing the gain of the stage and ensuring correct operation even if one of the two inputs is floating (or zero). The output voltage of the stage is zero on one of the output terminals and is the larger voltage between $V_{dd}$ and $V_{ss}$ on the other terminal. These voltages ensure that one of the two switches MC1 and MC2 is 'on' while the other is 'off'. Thus the substrate is correctly biased through the 'on' switch at the higher available voltage.

The gain of the stage of the order of

\[ A_v = \frac{y_{in} y_{out}}{y_{in} (y_{in} + y_{out})} \]

The dimensions of the transistors can be chosen to achieve a gain of a few hundreds, enough to guarantee a finite switching of the substrate voltage when the input differs from $V_{dd}$ by a few millivolts.

A possible drawback of the circuit can arise from the fact that the switching control circuit (and the substrate) is largely biased by the higher voltage source. If its series resistance is not negligible, the voltage drop across it generates oscillations if the input voltages of the comparator are close enough.

In order to avoid this problem, hysteresis in the comparator response must be introduced. It is obtained, as shown in Fig. 2, by four additional transistors MA1–MA4. One of the two

Fig. 1 Circuit diagram of comparator

Fig. 2 Circuit diagram of comparator with hysteresis

ELECTRONICS LETTERS 16th August 1990 Vol. 26 No. 17
transistors MA1 or MA2 is connected in parallel with M1 or M2 respectively through the switches MA3 and MA4 driven by the outputs. The connected additional transistor suitably unbalances the input differential pair, thus introducing the required hysteresis.

Experimental results: Two test circuits, one without hysteresis and the other with hysteresis, were integrated with a 3 μm CMOS p-well technology. Fig. 3 shows the microphotograph of the comparator with hysteresis used for the substrate bias of a complex system. The dimensions were chosen to give a gain of 50 dB and a hysteresis of 10 mV. Fig. 4 shows the substrate bias for the comparator (a) without and (b) with hysteresis. \( V_{BB} = 3.5 \text{ V} \) and the input voltage varies from 3.2 V to 3.8 V.

![Microphotograph of comparator with hysteresis](image)

Fig. 3 Microphotograph of comparator with hysteresis

![Graph of substrate bias against input voltage](image)

Fig. 4 Substrate bias against input voltage

(a) Comparator without hysteresis

(b) Comparator with hysteresis

The measurements show that, as expected, in the first circuit the substrate is biased to the higher voltage between \( V_{BB} \) and \( V_{DD} \) when they are sufficiently different. In the transition region the substrate voltage is not well defined because the circuit breaks into oscillation.

With hysteresis (Fig. 4b) this effect disappears and the substrate bias definitely switches when \( V_{BB} = V_{DD} + \frac{1}{2} V_{BB} \). A closer look at the experimental results (Fig. 5) allows evaluation of the hysteresis range. The measured value was 9 mV, in good agreement with the designed value of 10 mV.

Conclusions: A suitable circuit for the switching of substrate or well bias when the input voltage exceeds the supply has been presented.

![Graph showing substrate bias against input voltage for the comparator with hysteresis](image)

Fig. 5 Substrate bias against input voltage for the comparator with hysteresis: detail of the transition region

The use of a comparator with hysteresis has been shown to be the best solution in order to avoid oscillations.

The circuit has been successfully used for the substrate bias of a complex integrated system.

U. GATTI
V. LIBERALI
F. MALOBERTI

Department of Electronics
University of Pavia
27100 Pavia, Italy

P. O’LEARY

Joanneum Research
Steinergasse 17
8010 Graz, Austria

References

1. GRAY, P. R., and MEYER, R. G. 'MOS operational amplifier design—A tutorial overview', IEEE J. Solid-State Circ., 1982, SC-17, pp. 969-982

2. GREGORIAN, R., and TIMIR, G. 'Analogue MOS integrated circuits for signal processing' (Wiley and Sons, New York, 1996)


OPTIMUM FACET REFLECTIVITY FOR HIGH SPEED LASERS

Indexing terms: Lasers and laser applications

The issue of optimum facet reflectivity for large bandwidth semiconductor lasers is addressed. The laser facet reflectivity is chosen for maximizing the relaxation oscillation frequency, by optimization of the photon lifetime and maximum obtainable intracavity photon density. The optimum mirror reflectivity also depends on the relative importance of photon density-induced facet damage, parasitic leakage, heating, and gain saturation. In practice, we find both theoretically and experimentally, that higher mirror reflectivities can result in higher modulation bandwidths. The issue of optimum mirror reflectivity is also of special interest for surface emitting lasers where the cavity length is very short but the mirror reflectivity is very high.

Introduction: High speed semiconductor lasers are important for new higher bit rate digital communications systems, microwave and millimetre wave analogue transmission systems, optical interconnects and instrumentation. A current research need is to increase the bandwidth of semiconductor lasers beyond the present limit of around 20 GHz. As researchers succeed in fabricating low capacitance laser structures whose bandwidths are not limited by electrical parasitics, the central