So the error correcting signal \( -E_{j}(-v_{0}) \) is obtained at the output terminal of the inverter and the error detection alarm is turned out by G4.

If the decoder works for error correction only, we send the 'run' to point (c) and 'lock' to point (c/d) to switch on G2 and switch off G1 and G3. The gate B, at this moment, becomes a pure majority gate because the majority bound for error correction only is \( \left\lfloor J/2 \right\rfloor + 1 = \left\lfloor d_{\text{min}}/2 \right\rfloor + 1 = t_{1} + 1 \). The error correcting signal is turned out from gate B and sent to the inverter through G2. No alarm appears at the output of G4.

Another part of enhancement corresponding to original decoder is a k-stage buffer, considering that the decoded information could be sent to the user only after a whole decoding procedure is completed because the decoder, in the 'c/d' state, must stop and all information decoded is invalid provided even one error detection alarm shows up.

**Example:** Consider the \((15, 7)\) cyclic code over \(GF(2)\) with the parameters of \(d_{\text{min}} = 5\) and \(J = d_{\text{min}} - 1 = 4\), we choose \(t_{1} = 1\) and \(t_{2} = 3\). The generating polynomial \(g(x)\) and parity-check matrix \(H\) are

\[
g(x) = 1 + x^4 + x^5 + x^7 + x^8
\]

\[
H = \begin{bmatrix}
000000001101000 \\
010000000110100 \\
001000000110100 \\
000100000110110 \\
000010000110111 \\
000001000110111 \\
0000001001100011 \\
0000000101100001
\end{bmatrix}
\]

By the linear combinations of eight row vectors of \(H\), we obtain four row-space vectors orthogonally checked on the 14th bit of the code such that

\[
w_0 = h_1 = (000100000001101)
\]

\[
w_1 = h_0 + h_2 = (001100000001001)
\]

\[
w_2 = h_0 + h_2 + h_5 = (1001000100000001)
\]

\[
w_3 = h_1 = (000000001100001)
\]

When decoding, four parity-check sums orthogonal on \(e_{14}\) are produced by the calculations between received vector \(r\) and \(w_0 \cdots w_3\) such that

\[
A_0 = w_0 \cdot r = e_3 + e_{11} + e_{12} + e_{14}
\]

\[
A_1 = w_1 \cdot r = e_1 + e_3 + e_{11} + e_{14}
\]

\[
A_2 = w_2 \cdot r = e_0 + e_2 + e_6 + e_{14}
\]

\[
A_3 = w_3 \cdot r = e_3 + e_8 + e_{10} + e_{14}
\]

For \(Hr^T = s\), the parity-check sums can also be represented as

\[
A_0 = w_0 \cdot r = s_3
\]

\[
A_1 = w_1 \cdot r = s_1 + s_3
\]

\[
A_2 = w_2 \cdot r = s_0 + s_2 + s_6
\]

\[
A_3 = w_3 \cdot r = s_3
\]

So the hardware circuit presented in Fig. 3 can build a one-step majority-logic decoder with the error correcting capacity of one and error detecting capacity of three.

**Discussion:** The decoding algorithm and pertaining decoder of linear one-step MLD codes over \(GF(q)\) used for both error correction and detection were investigated. The decoding algorithm presented can be easily extended to \(L\)-step MLD codes because the decoding method for \(L\)-step MLD codes is finally, through certain steps of orthogonal processing, reduced to that of one-step MLD codes. So we may directly use the new decoding algorithm in the last step of \(L\)-step majority-decoding; i.e., to replace the majority gate of its last step by two decision and other control gates.

![Diagram of 8 stage syndrome storage circuit](image)

**Fig. 3** Decoder of \((15, 7)\) code in 'c/d' state

The performance analyses of this algorithm and the computation of probability of undetected error after decoding, etc., still remain to be investigated.

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19th July 1990

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**BIT STREAM ADDER FOR OVERSAMPLING CODED DATA**

**Indexing terms:** Adder circuits, Sigma-delta modulation, Delta modulation, Oversampling

A method of adding oversampling coded data streams is presented. The available oversampling is used to add the spectrums with the minimum of degradation in the band of interest.

**Introduction:** In many applications where oversampling coded data is to be processed, e.g., sigma-delta modulation, it is necessary to add or subtract two one-bit data streams, maintaining only one-bit data at the output.
A one bit adder is shown in Fig. 1. The addition of \( A \) and \( B \) results in both a 'sum' and 'carry'. It is obvious that a one-bit output word is inadequate to describe all combinations of the two one-bit input data streams. If only the 'sum' bit is used at the output, then the adder is reduced to a simple EXOR gate. Unfortunately, with this solution it is not possible to differentiate between addition and subtraction. This solution also results in serious intermodulation between the two data streams. The use of the 'carry' as output leads to a reduction in the useful dynamic range. If one of the input bit streams remains at zero then the other channel can never contribute to the output.

The output of the adder has three possible output states: 0, 1 or 2. In the case of subtraction the possible states are \(-1, 0, 1\). A solution for representing the three states with one bit has been proposed by Engel. The solution uses the one bit to represent the two possible extreme points i.e., 0, 2 or \(-1, 1\) and a sequential alternation of the output bit to represent the intermediate level. This method does not take advantage of the available oversampling to construct a more optimum solution.

**Bit stream adder using oversampling:** Since the input data streams are oversampling coded, it is possible to use oversampling based noise shaping to reduce the error caused by the bit stream addition. The solution proposed here is shown in Fig. 2. The output of the circuit is the carry of a full adder. The sum bit, which can not be fed directly to the output is stored and added to the following input bits.

The circuit is described by the following z-domain equation:

\[
output(z) = BS(z) + BS(z) - (1 - z^{-1}) \text{sum}(z)
\]

where

\[
z = e^{-j\omega t}.
\]

This is equivalent to first order sigma-delta noise shaping where the 'sum' from the adder corresponds to the quantisation error. For low frequencies

\[
\omega \rightarrow 0 \Rightarrow z^{-1} \rightarrow 1
\]

Then the output is given by

\[
output(z) = BS(z) + BS(z)
\]

Thus, for low frequencies the output is a perfect representation of the addition of the two input data streams.

To verify the operation of this circuit, a computer simulation based on a discrete time model was performed. Two sigma-delta coded bit streams sampled at 255 kHz representing sine waves of 990 Hz and 525 Hz were added using the proposed circuit. Fig. 3 shows a detailed plot of the composite spectrum at the output of the adder. From the plots it can be seen that the circuit causes no significant reduction in the signal to noise ratio. More importantly, there are no inter-

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**DIVERSE ROUTING IN WAVELENGTH SELECTIVE NETWORKS**

**Indexing terms:** Optical switching, Networks

Diverse routing of wavelength division multiplexed signals is demonstrated in one transmission path of a wavelength routed star network operating in the 1.55\(\mu\)m transmission window at 650 Mbit/s. The network is demonstrated with six wavelengths accessing four output paths from the central node. Route switching of high wavelength channels is achieved using aluminium co-doped erbium fibre amplifiers.

**Introduction:** A wavelength routing network\(^1,2\) uses wavelength to define a path through an optical network. The path may be fixed or switched and a variety of structures can be formed\(^2\) using suitably interconnected wavelength division multiplexing (WDM) elements. Small scale unamplified networks carrying 650 Mbit/s over 50 km are feasible\(^3\) but for greater ranges optical amplification is required to overcome the loss introduced by the multiplexers. This type of network offers a high degree of optical interconnectivity and is particularly suited to core telecommunication networks where large traffic capacity is required between a group of switching centres. A means of providing path protection is particularly important because the traffic carried over any given fibre or