Direct digital synthesis applied to modulators for data communication

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This paper presents an introduction to direct digital synthesis. The application of this synthesis technique to modulators for data communication is explained. Modulators for frequency shift keying, phase shift keying, amplitude shift keying and quadrature amplitude modulation are presented.

1. Introduction

In data communication circuits which work over a telephone line some form of data modulation is required. Different modulation techniques are used depending on the data transmission speed. For low speed communications frequency shift keying (FSK) is the preferred modulation form (see Table I). FSK has the advantage of not requi-

<table>
<thead>
<tr>
<th>Speed</th>
<th>Duplex</th>
<th>CCITT</th>
<th>Modulation</th>
</tr>
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<tbody>
<tr>
<td>300</td>
<td>Full FDM</td>
<td>V.21</td>
<td>2-FSK</td>
</tr>
<tr>
<td>1200</td>
<td>Half FDM</td>
<td>V.23</td>
<td>2-FSK</td>
</tr>
<tr>
<td>1200</td>
<td>Full FDM</td>
<td>V.22</td>
<td>4-DPSK</td>
</tr>
<tr>
<td>2400</td>
<td>Half FDM</td>
<td>V.26</td>
<td>4-DPSK</td>
</tr>
<tr>
<td>2400</td>
<td>Full FDM</td>
<td>V.22bis</td>
<td>16-QAM</td>
</tr>
<tr>
<td>2400</td>
<td>Full EC</td>
<td>V.26ter</td>
<td>4-DPSK</td>
</tr>
<tr>
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<td>Half EC</td>
<td>V.27</td>
<td>8-DPSK</td>
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<td>Full EC</td>
<td>V.32</td>
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<td>V.29</td>
<td>16-AM/PM</td>
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<td>V.32</td>
<td>32-QAM</td>
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<tr>
<td>14400</td>
<td>Half EC</td>
<td>V.33</td>
<td>128-QAM</td>
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TABLE I Modern standards and modulation method used (FDM refers to frequency division multiplexing and EC for echo cancelling)

ing clock extraction for the synchronization in the receiver, but the bit error rate for a given signal-to-noise ratio (SNR) is high. A modified form of FSK called “Minimum Shift Keying” (MSK) improves the bit error rate for FSK. “Phase Shift Keying” (PSK) and “Differential Phase Shift Keying” (DPSK) offer a better bit error rate for the same SNR as the FSK at the cost of a somewhat more complicated receiver. For high speed data communication “Quadrature Amplitude Modulation” (QAM) is used. QAM unfortunately requires a very complicated receiver.

The modulators used in previous systems have usually relied on switched capacitor sine wave generators [1] which use a clock frequency of approximately 16 times the required frequency. Such a modulator generates mirror frequencies little more than one decade above the base band. Depending on the modulation scheme used, a precision post-filter may be required to remove the unwanted frequency components. These filters are not trivial and usually require significant silicon area and are sensitive to process variations.

Using “Direct Digital Synthesis” (DDS) [2] – [4] it is possible to utilize the speed of modern silicon processes to simplify the analogue structures required and reduce the design complexity of data communication circuits.

The frequencies needed for the transmission of data over a telephone line are in the range from 300 Hz to 3.4 kHz. This paper describes an efficient way to generate the signals required for the modulation in data transmission. The proposed technique makes use of DDS implemented in CMOS technology. Modern CMOS processes allow the use of clock frequencies in the megahertz range; thus the mirror frequencies which are generated are in a range where the unwanted components are easily removed. Moreover, the use of a high oversampling ratio gives benefits in the simplifications of the digital-to-analogue converter. For most applications it is sufficient to use a first-order sigma-delta converter [4].

2. Direct digital synthesis

Figure 1 shows the block diagram of a direct digital synthesizer. The synthesizer consists of two

![Fig. 1. Basic direct digital synthesizer.](image)
blocks, the phase accumulator and the sine ROM. The phase accumulator is incremented at each clock cycle by the phase increment at the input. The output of the accumulator represents the phase of the desired sine frequency. When the accumulator overflows, it performs a modulo function, the remainder is then added to the phase increment during the next clock cycle. This ensures the long-term precision of the generated frequency. The sine ROM converts the phase output of the accumulator to a sine amplitude in digital form. The output of the direct digital synthesizer is a digital sine wave sampled with the frequency \( f_s \) and quantized to \( n \) bits.

The frequency generated by the synthesizer is given by the following equation

\[
f_{\text{out}} = \left( \frac{\text{Phase Inc}}{2^m} \right) f_s, \tag{1}
\]

where \( m \) is the number of bits in the accumulator and \( f_s \) is the clock frequency.

The minimum frequency resolution can also be derived from eqn. (1) and is given as

\[
f_{\text{res}} = \left( \frac{1}{2^n} \right) f_s. \tag{2}
\]

Equation (2) can be rearranged to give the required accumulator for a given frequency resolution

\[
m = \log_2 \left( \frac{f_s}{f_{\text{res}}} \right) \tag{3}
\]

For example, if the frequency 1.1 kHz is to be generated with 1% accuracy from a 3.58 MHz clock then the accumulator must have at least 19 bits. For large accumulators the use of pipelining should be considered to avoid propagation delay problems [2].

The SNR of the generated sine wave can be calculated from the bit width of the ROM data. The following calculation assumes that the sampling quantization and the generated sine wave are not correlated.

\[
\text{SNR} = (6.02n + 1.7) \text{ dB} \tag{4}
\]

For the transmission of data over the telephone network relatively low SNRs are required. The SNR required for DTMF [5] dialing is -25 dB. Such a SNR can be achieved with very few bits making the required ROM very simple. A sine ROM with five bit address and five bit data, see Fig. 2, gives a SNR of -31.72 dB; this is more than sufficient and leaves some room for noise in other parts of the system. The symmetry of the signal can be utilized to further reduce the ROM size.

When designing a digital synthesizer some consideration should be directed to the output spectrum. The spectra of three different sine waves generated from adjacent codes are shown in Figs. 3(a)-3(c). The spectra show dramatic differences. Particularly the spectrum of Fig. 3(b) does not resemble an analogue sine in the presence of noise. The spectrum consists of the base signal and only harmonic components. The spectrum of Fig. 3(b) can cause convergence problems with some echo cancelling algorithms [6]. The different spectra are caused by the correlation between the quantization error and the generated sine wave (a similar problem is observed with first order sigma-delta converters). The sine generated in Fig. 3(a) is an exact subharmonic of the sampling frequency. Such frequencies generate spectra with artificially high harmonic components.

The correlation between the quantization error and the generated frequency can be removed by the addition of a random phase component to the sine wave. This is similar to the addition of amplitude dithering (or spectral distribution functions) with sigma-delta converters [7]-[10]

\[
\text{Out} = \sin(\omega t + \phi) \tag{5a}
\]

where \( \phi \) is the random phase component.

\[
\text{Out} = \sin(\omega t) \cos(\phi) + \cos(\omega t) \sin(\phi) \tag{5b}
\]

For small \( \phi \) the following approximation can be made

\[
\text{Out} \approx \sin(\omega t) + \phi \cos(\omega t) \tag{5c}
\]

\[
A \quad B
\]

Equation (5) describes the output signal with the addition of a small phase dither. The output signal with the addition of a small phase jitter is described by eqn. (5). The output consists of the desired sine frequency (portion A) and an amplitude modulated random component (portion B). The amplitude of the dither is a maximum at the zero crossings of the sine wave. This decorrelates the generated frequency and the sampling frequency, reducing the distortion. The amplitude of the added noise is zero at the maximum amplitude of the sine wave. This results in a lower noise power compared with amplitude dithering for a given decorrelation factor.
Fig. 3. Direct digital synthesis of three differing sine waves: (a) spectrum of example (a); (b) spectrum of example (b); (c) spectrum of example (c).
Figure 4 shows a digital synthesizer with phase dithering. The dither sequence is generated using a linear feedback shift register [11]. A maximum length PN sequence is chosen to guarantee a uniform probability density function for all codes. This is necessary to maintain the same average frequency with the addition of phase dithering. This random sequence used has also a pseudo white spectrum in the required base band. This avoids the generation of intermodulation terms.

![Digital synthesizer with phase dithering](image)

Fig. 4. Digital synthesizer with phase dithering.

Figure 5 shows the spectrum of the same signal as Fig. 3(b) but with the addition of 1% phase dithering. The output spectrum is now closer to a sine wave in the presence of noise. The harmonic components due to the correlated quantization noise have now been spread over the spectrum.

3. Digital-to-analogue conversion
The digital sine wave generated by the synthesizer must be converted to analogue form before being transmitted over a telephone line. For this purpose a digital-to-analogue converter is required. Because only medium resolution is required many possible architectures for the data conversion are possible. The typical resonator frequencies used in telephone applications are in the 2–4 MHz range and the frequencies which must be generated are in the 0.3–3.4 kHz range. This high oversampling ratio of approximately 1000 would seem to make an oversampling converter the most logical choice because of their simple architecture.

The most popular form of oversampling converter in recent years is the sigma–delta converter (ΣΔ). These converters use one bit quantization and a noise shaping function to redistribute the noise power in the spectrum. This results in a simple architecture without precision analogue components. Equation (6) shows the general noise shaping function for an nth order sigma delta converter

\[
\text{Out}(z) = [\ln(z) - (1-z^{-1})^n E(z)]
\]

where \( E(z) \) is the quantization error.

Analysing eqn. (6) shows that the quantization noise at low frequencies, i.e. \( z^{-1} \rightarrow 1 \), is reduced. At DC there is theoretically no quantization noise. Whereas the noise at higher frequencies is amplified, this increased noise at higher frequencies is then removed with a post-filter, resulting in a converter with high resolution for large oversampling ratios.

With considerable effort and with many assumptions [13] it is possible to calculate the SNR ratio for a sine wave signal given the oversampling ratio based on eqn. (6). Performing this calculation for a first order converter results in the following equation

![Spectrum of the same sine wave as example 3(b) but with 1% phase dither](image)

Fig. 5. The spectrum of the same sine wave as example 3(b) but with 1% phase dither.
SNR = \left[ 30 \log (R_a) \right. \\
\left. + 10 \log \left( \frac{X_{\text{max}}}{\Delta_s - X_{\text{max}}/2} \right) - 5.17 \right] \text{dB} \quad (7)

This equation is also valid for multi-level \( \Sigma\Delta \) converters. A further simplification of eqn. (7) is possible to derive an equation suitable for estimating the converter performance. This equation is only valid for one bit quantization

\[
\text{Res} (\Sigma\Delta_a) = [1.5 \log_2 (R_a)] \text{ Bits} \quad (8)
\]

Equation (8) can now be used to estimate the requirements for the present application. An oversampling ratio of about 1000 is available. This would give a theoretical resolution for the digital-to-analogue converter of approximately 15 bits. This is considerably better than the specification required in this application. As a result the sampling rate can be decreased to save power. By turning eqn. (8) around it is possible to calculate the minimum oversampling required for a given application. For the circuits proposed here, 5-6 bits of resolution are required; this would require a minimum oversampling ratio of approximately 16. Such a low rate will be applied as it is desired to keep the mirror frequencies in a region where they can be removed with a simple continuous time post-filter.

Behind these calculations are many assumptions about the nature of the quantization noise. One major assumption is that the quantization noise is not correlated with the input signal, i.e., that quantization is a linear process. This is an assumption which may be true for random signals, but is not necessarily fulfilled for a pure sine wave [12], [13]. This leads to considerable differences between the theoretical calculations based on eqns. (6) and (7) and what is seen in practice. Figure 6 shows the output spectrum of a first order sigma delta converter when driven by a pure sine wave, with an oversampling of 100. The spectrum has discrete spectral lines which are caused by the correlation between the input signal and the quantization noise.

Similar to the digital synthesizer, this correlated noise can be removed with the addition of amplitude or phase dithering [9]. In the case presented here this correlation is automatically removed by the pseudo random nature of the data being transmitted by the modems. Most modems use data scramblers to avoid low frequency components on the telephone line. These scramblers also guarantee a pseudo random data sequence. Some form of phase or amplitude dithering should be used in applications where only one fixed frequency is generated.

Figure 7 shows an implementation of a first-order sigma-delta digital-to-analogue converter. The modulator bit slice is the same as for the phase accumulator. This is advantageous for a full custom layout. The low pass post-filter is based on a Sallen and Key architecture. This structure is the most suitable for monolithic integration. The passband gain of such a filter is only dependent on the operational amplifier open loop gain and not on element matching. Secondly, the resistors carry no current in the passband, which permits the use of non-linear resistors for monolithic integration without degrading performance.

![Fig. 6](image_url)

\textit{Fig. 6. The spectrum of a first-order sigma-delta converter.}
4. Frequency shift keying
With frequency shift keying (FSK) the frequency of the carrier is modulated by the data. FSK is often used where non-linear channel distortion is present, because only the zero crossings have to be maintained to determine the frequency being transmitted. The fact that FSK can be demodulated with non-coherent methods makes it suitable for applications where simple receiver hardware is important or where minimum power consumption is required.

For binary FSK only two frequencies are used. The first frequency represents a one and the second frequency the zero, see Fig. 8. The CCITT V.21 300 b/s voice band modem [14] uses binary FSK with the frequencies 1080 ± 100 Hz for transmission in one direction and 1750 ± 100 Hz for transmission in the other. The V.21 modem was developed at a time when the simplicity of the receiver was important.

A frequency shift modulator is easily implemented with DDS. Figure 9 shows the block diagram for a binary FSK modulator. The two desired frequencies are coded as their respective phase increments as required for the accumulator. The binary data which is to be transmitted is then used to select the corresponding phase increment. Only the rate of phase accumulation is changed, consequently there is no discontinuity in the output amplitude. This is advantageous as discontinuities in the transmitted amplitude generate out of band noise.

Another advantage of FSK is the constant envelope modulation technique, i.e. the carrier amplitude always remains constant. This makes it possible to design the analogue amplifiers and post-filters, optimized for one amplitude.

The simplicity of FSK is offset with one major disadvantage, the SNR performance for low dimensionality is 3 dB lower than for antipodal amplitude modulation of antipodal phase modulation. If, however, many bits are transmitted per baud, i.e. high signal dimensionality, then the performance of FSK can be superior to that of non-orthogonal modulation techniques. We have taken advantage of this property to develop a FSK modulator with 10 bits per baud (1024 dimensional transmission space) in a 2 μm N-well CMOS process. The circuit requires less than 1 mm² with all required filtering. The circuit is designed for a remote measurement system where power consumption is a major restriction. The simplicity of this transmission circuit and required demodulator made it possible to implement the complete measurement and data transmission system on one chip.

5. Modifications to FSK
A second disadvantage of FSK is the widely spread spectrum at the output. The wide spectrum is caused by the jumps from one frequency to the next. The change is phase continuous but the rate of change is discontinuous. This discontinuity causes considerable in and out of band noise. A method called “Tamed FSK” was proposed by F. de Jager and Dekkers to solve this problem. With this technique the modulator changes gradually from one frequency to the next.
A Tamed FSK can be generated with DDS simply by placing an interpolation circuit before the phase accumulator. The interpolator generates the required intermediate values to ensure that the frequency transitions are smooth. This technique results in a considerable improvement in the spurious noise performance of the modulator. Figure 10 shows a simulated comparison of the output spectrum of a Tamed FSK and a normal FSK modulator, while both transmit the same data.

A well-known application of FSK is DTMF [5] dialing. With DTMF dialing two frequencies are transmitted simultaneously. The transmitted frequencies are split into two groups, an upper frequency group containing four frequencies and a lower group of four. One frequency is transmitted from each group. A complete description of the DTMF generator is given in ref. 16. The 16 possible combinations are then used to represent the telephone number which is being dialled. The frequency synthesizer can be modified to generate
two frequencies simultaneously in an interleaved mode, see Fig. 11, simply replacing the \(z^{-1}\) of the accumulator by a \(z^{-2}\) and alternating the input to the accumulator. Such a DTMF generator has been developed at AMS using a 2 \(\mu\)m N-well CMOS process and requires 1.3 mm\(^2\), using a standard cell approach to the layout. Figure 12 shows a measured spectrum from the DTMF.

6. Phase shift keying

Phase shift keying (PSK), in particular DPSK, is very popular in medium speed modems because of its spectral efficiency [6], [13]. The generation of PSK is also possible with DDS.

There are two possibilities to add phase modulation to a fixed frequency generated by a digital synthesizer: the output of the accumulator represents the phase of the generated sine wave. Adding or subtracting a phase component to this point modulates the phase of the sine, see Fig. 13. The disadvantage of this solution is that it requires an additional adder. This adds to the group delay of the synthesizer a feature which is not desirable for echo-cancelation applications.

A second solution is possible when a relatively high oversampling ratio is being used. The fixed phase increment for the generation of the carrier frequency is then restricted to the lower bits of the accumulator. The MSBs are free for the addition of the required phase modulation. The MSB of the accumulator corresponds to an angle of \(\pi\).

Using this information it is possible to define a phase transition table. To generate 4-DPSK the two most significant bits of the accumulator must be manipulated during one clock cycle. The bit manipulation is extremely simple, it requires only one inverter. see Table II.

<table>
<thead>
<tr>
<th>Dbit</th>
<th>Phase change (V.22)</th>
<th>MSB</th>
<th>MSB-1</th>
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<tr>
<td>00</td>
<td>90</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>270</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>180</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

7. Amplitude modulation

The amplitude of the sine wave can be modified by varying the reference voltage applied to the output switches. The required references can be generated with a simple resistor chain. The transmission data is then used to select the required output amplitude. This is a very simple implementation of an amplitude modulator but is only practical where the number of amplitudes required output amplitude. This is a very simple communication.

The modulator presented here can be extended to quadrature amplitude modulation. If the ROM is alternately selected to be sine and cosine, then

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Fig. 12. The measured spectrum from the DTMF.
the samples coming to the output structure are interleaved quadrature signals of the same frequency. If the vector components are alternately applied to the voltage reference then a quadrature amplitude modulated signal results at the output.

8. Conclusions
The feasibility of combining DDS with first-order sigma-delta modulation to give simple data modulators has been demonstrated in this paper. This technique, due to the regular structures used is particularly suited for monolithic integration. Circuit configurations for all major data modulation techniques have been presented (FSK, PSK, DPSK, ASK, QAM) as well as an integrated FSK modulator with a frequency range from 300 Hz to 3000 Hz with 1 Hz resolution. The FSK modulator was integrated in a 2 μm N-well CMOS process and required 0.6 mm². The application of this technique to DTMF generation has also been demonstrated.

9. References
Biographies
For the biography of Paul O'Leary see the Journal of Semicustom ICs, Vol. 6, No. 4, June 1989, p.18.

Helmut Horvat was born in Kapfenberg, Austria on August 13, 1960. He received the Diploma degree from the Technical University of Graz, Austria in 1987. During 1986 he did his Diploma Thesis on CMOS Op. Amps.OTAs in cooperation with Austria Microsystems (AMS) in Graz. In summer 1987 he joined the analogue group of AMS, where he was involved in the design of analogue library cells and switched capacitor filters. In 1989 he changed to the full-custom group and currently works on telecom systems and oversampling converters.

Professor Franco Malberti was born in Parma, Italy, on December 10, 1945. He received the Laurea degree in physics in 1968 from the University of Parma. From 1968 to 1969 he was a research assistant with the University of L'Aquila. In 1969 he joined the Department of Electronics, University of Pavia, Pavia, Italy where he is currently a Professor. His teaching and research interests include the general areas of microelectronics, analogue signal processing and analogue/digital converters. Professor Malberti is a member of the Associazione Elettrotecnica Italiana (AEI).