An Integrated CMOS Telephone Line Adapter

OLUF ALMINDE
Austria Mikro Systeme International GmbH, 8141 Unterpremstätten, Austria

UMBERTO GATTI, VALENTINO LIBERALI, FRANCO MALOBERTI
Department of Electronics, University of Pavia, 27100 Pavia, Italy

PAUL O’LEARY
Joanneum Research, Steyrergasse 17, 8010 Graz, Austria

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Abstract. A novel fully CMOS circuit for electronic telephone line adaption is described. In the on-hook state the circuit operates in micropower condition, dissipates only 5 μA, and is capable of generating the supply voltage required for retention of data stored on external RAM. In the off-hook state the circuit is boosted into the normal operation mode and is able to drive external bipolar transistors to synthesize the line impedance. The dc and the ac line impedences are set with external components, thus permitting the fulfillment of different PTT specifications. The circuit also performs line signal extraction and transmission, both for voice and DTMF. The dc line voltage is monitored, and a supervision block generates a precise reset signal when the line voltage drops out. The circuit has been integrated in a CMOS P-well 3-μm double-poly single-metal technology; the silicon area is 6 mm².

1. Introduction

The recent trend in telephone set integration was toward single-chip solutions [1], [2]. However, these solutions relied on complex technologies, required a large silicon area, and also sacrificed flexibility in system implementation, making it difficult to build telephones with different features (display drivers, nonvolatile number storage, etc.). Moreover, and more importantly, the single-chip solutions neglected the electronic line interface problem.

In order to identify the more suitable architecture capable of fulfilling different PTT specifications and also to solve the line adaption problem in the best way, the chip described in this paper was designed and integrated.

A first interesting characteristic of the circuit is the possibility of a permanent connection to the line, even when on-hook. This feature allows the implementation of an electronic switch control without physically commuting from on-hook to off-hook. In the standby condition the circuit is able to generate a mask programmable regulated voltage for the retention of data stored on external RAM, obtained by a micropower band-gap reference and a micropower voltage regulator. In the off-hook mode, all the amplifiers are powered up and those used in the on-hook condition are boosted from micropower mode into normal mode, thus improving the slew rate characteristics of the circuit.

Moreover, for countries where no on-hook leakage current is permitted, the power can be supplied to the chip with an external battery. In this case, two possible supply sources must be used. The substrate must always be biased to the higher voltage of the circuit. In the on-hook mode the line voltage is usually larger than the battery voltage, so the line voltage must be used only to bias the substrate while the battery is powering the circuit. By contrast, in the off-hook mode, to prevent battery discharge, the line must supply the circuit while the battery can be used only to bias the substrate. All these problems were solved with suitable automatic switching of the power supplies [3].

It is known that one of the main limitations to the use of CMOS technology in telephony concerns circuit protection against overvoltages. The proposed system uses a new protection scheme which requires the use of an external MOSFET. The resulting protection is robust enough to allow the use of CMOS circuits, thus opening the way to a fully CMOS telephone set [4].

2. Circuit Description

Figure 1 shows the block diagram of the system. The protection circuit is made of an external depletion MOSFET, a Zener diode, and a bias resistance. If the voltage at node 1 exceeds the Zener voltage, the MOSFET is turned off and overvoltages from the line
are rejected. The dc and ac line impedances are defined by the loop control feedback $A_1$, $Q_1$, and/or $Q_2$-external network. The use of external components is essential to a versatile line adaption circuit, as telephone companies have different specifications in each country for their line terminations. If the loop gain is large enough, the value of the small resistance $R_L$ is multiplied by two distinct dc and ac factors, and the circuit impedances $Z_{dc}$ and $Z_{ac}$ result as follows:

$$Z_{dc} = R_L \frac{R_3 + R_1}{R_3}$$  \hspace{1cm} (1)

$$R_{ac} = R_L \frac{Z_3 + Z_2}{Z_1}$$  \hspace{1cm} (2)

If $R_1 \ll R_3$ and $R_2 \ll R_1$, the ac impedance (for $s \rightarrow \infty$) is

$$Z_{ac} = R_L \frac{R_1 + R_2}{R_1}$$  \hspace{1cm} (3)

The block CONT controls the partitioning of the line current between the external load (the pin VCC) and the bipolar transistor $Q_1$, which shunts the redundant current to ground. To ensure that no dc current flows through the external path $R_1$-$R_3$ in the on-hook condition, the CMOS transistor connecting pin LS1 to ground is opened. During the off-hook state the same transistor is used to control an output buffer. Thus, the reference voltage VREF1 is replicated at pin LS1. This behavior allows the introduction of the desired offset into the dc line characteristic. Pin LS2 is disconnected from ground during the on-hook condition in order to avoid a fast discharge of the capacitors of the external network. This feature is important during the short periods associated with pulse dialing.

With commercial bipolar transistors the circuit is capable of draining up to 120 mA from the line to the telephone. This value is much larger than any standard requirement.

The use of the four-input amplifier $A_1$ (described in detail in Section 3) allows the combination of the line impedance control feature with the transmission of two different signals at the same time. They could be, for example, the voice (TX) and a DTMF signal (MF). The gain of the transmitted signals is approximately equal to the impedance gain given by $(Z_1 + Z_2)/Z_1$ if $Z_2 \gg R_1$.

The block DC EXTR and the external capacitor connected to the pin DC extract the dc component of the VL pin. This information is useful in estimating the
line current for the control of an external AGC on the transmit and receive amplifiers.

The received signal must be attenuated by a K factor and shifted around the 1.15-V reference voltage. In this way it is possible to drive an external loudspeaker correctly (RX pin) without using coupling capacitors. This function is obtained by a suitable use of another four-input opamp cascaded with a buffer (A3). The pin RX can be loaded with 1 kΩ and 100 pF.

The supply of external RAM memories even in the on-hook state requires the regulation of the line voltage with a minimum current consumption. The micropower band-gap voltage reference generates the 1.15-V reference and provides the bias current reference for micropower operation of the system.

Block VREF1 generates the voltage required at pins LSI and LS2 during off-hook operations of the circuit. Block VREF2 generates the stabilized VDD voltage for RAM supply.

The VB input is used for off-line power source (for example an external battery).

A reset circuit provides a precise monitoring of the level of the VDD power supply (pin RS). The reset time delay is set by an external capacitor and by the internal microcurrent source. The operational amplifiers used in the reset circuit also work in the micropower condition during on-hook operations.

The LOGIC CONTROL section provides all the required logic signals. The change from on-hook to off-hook is determined by a logic high signal applied to pin DP.

3. Four-Input Amplifier

The four-input amplifier (figure 2) is derived from the conventional two-stage operational amplifier with a pole-splitting compensation scheme. This block is known as a differential difference amplifier [5].

Two identical differential pairs are used in its input stage in such a way that the output voltage is an amplification of the superposition of the two differential inputs:

\[ V_{\text{out}} = A_v(V_{\text{IN,DIFF1}} + V_{\text{IN,DIFF2}}) \]  

(4)

The feedback loop tends to reduce to zero the quantity \( V_{\text{IN,DIFF1}} + V_{\text{IN,DIFF2}} \). Since the feedback control can be established only upon an input pair, the unbalance of the auxiliary pair is also reflected on one of the feedback pair. To guarantee a good distortion performance, it is necessary to allow an input unbalance equal to the maximum signal applied to the auxiliary pair. This feature is obtained by using input devices M1–M4 with relatively small W/L ratio.

Because the input voltages have low dc values (around 1.15 V), a complementary version of the circuit shown in figure 2 was implemented, in the receiving block, using p-channel input devices. In addition, since an output buffer was introduced to reduce the output impedance and to drive the load at pin RX, an improved internal compensation was also added.

4. Band-Gap Voltage Reference

In order to supply external RAM memories even in the on-hook state, it is necessary to generate a regulated voltage supply with a negligible current consumption (less than 5 μA). This function has been implemented by using a micropower band-gap reference and a micropower voltage regulator (figure 3). Both designed blocks are based on conventional architectures [6]–[8]. The micropower feature is simply obtained by using resistances in the megohm range. The encountered design problems concern two key points:

1. Is the \( I_f - V_{BE} \) characteristic of bipolar transistors in the submicroampere region still suitable for correct behavior of band-gap reference?

2. How should reliable high-value resistors be designed?

To answer to the first point, the current contributions in the close proximity of \( I_f = 0 \) were considered. The results show that severe limitations arise if \( I_f < 200I_{GR} \), where \( I_{GR} \) is the generation-recombination current. In the designed circuit, the emitter areas of the two bipolar transistors were 60 \( \mu \text{m}^2 \) and 480 \( \mu \text{m}^2 \), respectively. The worst-case GR current density for the process used (\( T = 100^\circ\text{C} \)) is \( 10^{-12} \text{ A/}\mu\text{m}^2 \). Thus, the worst-case GR current is around 0.5 nA. By using the above rule, it follows that the emitter current must be larger than 0.1 μA. In our design 0.5 μA (nominal case) was used.
The second point concerns the design of reliable high-value resistors. It is known that high specific resistance is obtained by well or pinched-well structures. Pinched-well structures have higher resistivity but display unacceptable variations depending on the fabrication process; thus, P-well resistances were used. In order to obtain a compact structure and to ensure insulation between neighboring elements, N⁺ diffusions around the P-well have been designed (figure 4). Thanks to this compact structure, the silicon area required to design a resistor as large as 3 MΩ is limited to 0.15 mm². The operational amplifier used in the band-gap reference does not need any slew rate enhancement because of its intrinsically static operation. The micropower reference current (0.5 μA) needed to drive the operational amplifier was obtained by using a self-biasing circuit. A 3-MΩ resistance between VDD and the substrate ensures the circuit start-up, since the substrate is always biased correctly. The two bipolar npn transistors were implemented with a standard CMOS technology, using the substrate as collector, the P-well as the base, and the n-channel source-drain diffusion as the emitter [9].

5. Substrate Bias Comparator

A specific problem of the designed circuit, common to all cases where multiple biases are foreseen, concerns the bias of the substrate. In our case either VCC (one bipolar saturation below VL) or the battery voltage VB can be used. Depending on operating conditions, VCC can be either larger or smaller than VB. For this reason it is necessary to monitor the two voltages and, of course, to bias the substrate to the higher one. This function is obtained by using the BIAS SWITCH block [3], shown in figure 5.

This circuit is a differential stage with two symmetrical parts directly powered by VCC and VB, respectively. The separate biasing allows correct operation of the comparator even if one of the two inputs is floating (or zero). Apart from this unconventional powering, the circuit composed of M1–M8 is a single-stage mirrored amplifier [10]–[12], whose inputs are VCC and VB shifted down in order to allow correct operation. The output voltage of the stage is zero on one terminal and the larger of VCC and VB on the other, ensuring that one of the switches M1 or M2 is on while the other
is off. Thus, the substrate is correctly biased to the higher available voltage. Since the BIASSWITCH and the substrate draw current from the higher voltage source, a voltage drop occurs if the series resistance toward the pad is not negligible, and oscillations can arise when the input voltages are close enough. In order to avoid this drawback, transistors MA1–MA4 are added to put the input differential pair off balance, thus introducing hysteresis in the comparator.

6. VDD Generator

The VREF2 block performs a combination of the functions of a switchover battery and a voltage regulator to generate VDD (figure 6). Voltage regulation is obtained by a conventional two-stage operational amplifier OP1 and two large MOS switches, MIY and M2Y. The stability of the voltage regulator is achieved by an external capacitor at the VDD pin. The input voltage of the regulator can be either VCC or VB. The choice between these two voltages is made by using amplifier OP2 in a Schmitt trigger (battery switchover function). Even in this circuit, high-value resistances are used in order to dissipate low power. Resistors R1 and R3 are also mask programmable: R1 regulates the desired VDD value in the range 2.5–5 V, while R3 sets the threshold of the trigger. The total resistance integrated for this block is about 5 MΩ.

7. Experimental Results

The described system has been fabricated with an industrial CMOS P-well 3-μm double-poly single-metal process. A microphotograph of the chip is shown in figure 7. The total die size is 6 mm².

The circuit was designed to operate with line voltage VL from 3.3 to 10 V. Thus, the threshold of the protection circuit must be set at 12 V. The function of the line adaption was tested with external component values capable of obtaining a dc impedance \( Z_{dc} \) of 60 Ω and an ac impedance \( Z_{ac} \) of 600 Ω. Figure 8 shows the voltage-current characteristic of the circuit as measured at node 1. The slope of this curve is around 60 Ω with an error of about 1%.

The line current is correctly partitioned between the external load through Q2 and the ground through Q1. The offset introduced into the dc line characteristic was 3.15 V ± 5%, as measured at pin LSI in different samples of the chip.
Fig. 7. Microphotograph of the chip.

Fig. 8. Voltage-current characteristic measured at node 1.

The transmission of the TX signal with an amplitude of 600 mV peak to peak and a frequency of 1 kHz exhibited a distortion below 0.5%, as shown in figure 9. Similar features were performed by the receiving amplifier.

Fig. 9. Measured power spectrum of the transmitted signal (frequency = 1 kHz, amplitude = 0.6 V_{pp}).
8. Conclusions

An integrated fully CMOS circuit for telephone line adaption has been presented. The multiple functions implemented by the chip allow it to satisfy the wide range of specifications and make the proposed circuit suitable for many applications (modern, telefax, etc.), fulfilling different PTT specifications. New circuit solutions have been experimentally verified. The performance obtained demonstrates that a single-chip CMOS version is feasible for the new generation telephone set.

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References

Oluf Alminde joined Austria Mikro Systeme International GmbH (AMS) in 1987 as telecom marketing engineer. His major responsibilities include the strategic marketing of AMS complete range of high-quality products for the telecommunications market, with a special emphasis on design and marketing of telephone ICs, including handset ICs for LD and MF dialing. Before joining AMS Mr. Alminde worked nine years with Alcatel Kirk where he was responsible for the design and development of telephone sets. Mr. Alminde's previous experience includes a degree in electronic engineering from the Technical College in Aachus, Denmark.

Umberto Gatti was born in Pavia in 1962. He graduated in 1987 with a Laurea degree in electronics engineering (summa cum laude) at the University of Pavia. In 1988 he joined the Department of Electronics of the same university, where he is currently working toward his Ph.D. in electronics and information engineering. His research interests are in the area of analog integrated CMOS circuits, particularly in continuous-time filter design. He is a student member of IEEE.

Franco Maloberti received the Laurea degree in physics from the University of Parma in 1968. He joined the University of L'Aquila, then the University of Pavia in 1969. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog applications. Dr. Maloberti has published more than 80 papers and holds 11 patents. He is coauthor with R. Soin and J. Frantzi of *Analog-Digital ASICs, Circuit Techniques, Design Tools and Applications*. He is a member of AEI (Italian Electrotechnical and Electronic Society) and a senior member of IEEE. He is currently professor of components and integrated circuits design at the University of Pavia, and is also head of the university's microelectronics laboratory.

Paul O'Leary was born in 1960 in Limerick, Ireland. He studied mathematics and electrical engineering at Trinity College, Dublin, where he graduated in 1982. In 1984 Mr. O'Leary received a masters degree in electronic engineering from Pd Eindhoven, Holland. From 1984 until 1987 Mr. O'Leary was at ITT Intermetal, Freiburg, Germany, where he worked on high-speed data converters for video applications and on direct digital synthesis. In 1987 he joined Austria Mikro Systeme, Unterpremstatten, Austria, where he was section manager of the analog circuits development group. Since September 1990 Mr. O'Leary has been in charge of a new research group at Joanneum Research, Graz, which works on electronic sensor interfaces. His interests are in data conversion, signal processing, and, in particular, oversampling based signal processing.

Valentino Liberati was born in 1959. He received the Laurea degree in electronic engineering from University of Pavia in 1986. From 1987 to 1990 he was with the INFN (Italian Nuclear Physics Institute), working on development and testing of low-noise electronics for particle detectors. In 1990 he joined the Department of Electronics of the University of Pavia, where presently he is assistant professor.