Design Tools for Oversampled Data Converters: Needs and Solutions

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The design of oversampled data converters imposes a set of specific trade-offs both at analysis and simulation levels. Because of their intrinsic non-linear nature, these circuits are difficult to analyze correctly using conventional theoretical tools. Furthermore, the accurate estimation of their major performance parameters requires their simulation over an extremely large number of clock cycles, a fact which imposes the use of dedicated behavioural simulators. This paper examines the specific needs in simulating switched-capacitor, noise-shaping data converters. We comment on the existing solutions presented in the literature as well as in the marketplace and compare them on the basis of three principal qualifying aspects: computation time vs. abstraction level and accuracy of the models; development time and cost vs. flexibility and user-friendliness; and finally, post-processing facilities available for evaluating system performance. In the final part of the paper we provide details concerning a general purpose and user-friendly behavioural simulator, which we developed (TOSCA [1, 2]). This tool represents a good trade-off between accuracy, flexibility, ease of use and computation time.

1. Introduction

A good and efficient simulation environment is presently considered an essential part of the mixed analogue–digital design process. Today's ASICs commonly put together complex analogue and digital circuits which, as known, require different simulation platforms. This increased activity in the area of mixed analogue–digital circuit design revealed some limitations in the available analogue simulators, especially because of the computation time required. One of the most important circuit blocks of a mixed signal processor is the data converter, which allows data to be converted between the digital and analogue domains. Recent trends in data converter design indicate that oversampling techniques are the most promising approach for implementing high-resolution analogue/digital interfaces, mainly because of their ability to trade speed for resolution. Given their relaxed requirements in terms of accuracy and matching between analogue circuit blocks, the use of these circuits turns out to be a good alternative for implementing data converters in monolithic systems which have to be integrated in silicon technologies that are optimised for digital circuitry [3–6].

To exploit fully the enormous potential oversampling converters represent, efficient methods are
building blocks like integrators, quantizers, delay elements, adders, multipliers, and digital decimators, which allow generic SC oversampled modulators and digital decimators to be built as a block-level network. When flexibility inside the integrator is important, a lower level of description was also considered. At this level the building elements are switches, capacitors and amplifiers, allowing users to analyse their own integrator topologies. The models developed for the building blocks allow the most relevant non-ideal parameters of the components to be considered, a fact which makes simulation results quite realistic. In the amplifier/integrator case, for instance, the model is able to take the effects of d.c. gain, bandwidth, slew-rate, offset voltage, output swing limitation and d.c. gain non-linearity into account [18]. The simulator contains post-processing routines that permit the circuits to be analysed extensively. Available facilities include the calculation of SNR for sinusoidal and d.c. signals, time and frequency probing of circuit node voltages as well as the calculation of their respective amplitude histograms. The simulator is very fast and takes less than 1 min to analyse 64 K sampling periods of common noise-shaping A/D converters.

Figure 3 gives an example of a two-stage, second-order, sigma–delta A/D converter and the corresponding input nlist for TOSCA. Figure 4 shows two possible simulation results that can be obtained with the tool.

4. Conclusions
An overview of existing simulation tools for the analysis of oversampled data converters has been
guide, Internal Report, Department of Electronics, University of Pavia, Italy, 1991.


