An Integrated CMOS Interface for Lambda Sensor

L. Civardi, U. Gatti, Student Member, IEEE, F. Maloberti, Senior Member, IEEE, G. Torelli, Member, IEEE

Abstract—Automotive pollution can be reduced by suitably controlling the mixture that is fed to the cylinders. This can be performed by means of a feedback loop including a lambda sond and a processing unit which controls the electronic fuel injectors. This paper describes a CMOS interface which adapts the output signal of a lambda sensor to allow its feeding into the processing unit. It provides a differential to a single-ended conversion with a good common mode rejection, a level shifting around a given reference voltage, and an accurate voltage gain. Both design considerations and the measurements performed on an integrated test structure are presented. The measured variation of the large-signal voltage gain for an input signal of 0 to 1 V is within ±5% when the input common mode voltage ranges from −1 V to 1 V with respect to the negative supply voltage. An output voltage with a precision within ±1 mV is obtained in the presence of an input voltage corresponding to the stoichiometric composition of the mixture.

I. INTRODUCTION

Air–fuel ratio (A/F) control in spark ignition automobile engines aims at reducing the volume of polluting gases (HC, CO, and NOx emissions) while achieving the best trade-off with fuel consumption. The excess-air factor λ is introduced, which is defined as the A/F normalized to the stoichiometric value [1]:

$$\lambda = \frac{\text{air/fuel (actual)}}{\text{air/fuel (stoichiometric)}}.$$  \hspace{1cm} (1)

The factor λ of the mixture fed to the engine has a dominant effect on exhaust-gas composition. A value of λ of approximately 1.1 is the optimum for best fuel consumption [2]. However, while CO and HC emissions are lowest at this setting, NOx emission reaches its maximum value. On the other hand, for λ = 0.9, the engine torque is at its maximum, but CO and HC emissions are higher.

In order to reduce noxious emissions, after-treatment of exhaust gases is necessary. A three-way catalytic converter (TWC) represents an efficient means of doing this. However, the conversion efficiency provided by a typical TWC (in terms of simultaneous conversion of all three main pollutants into harmless constituents such as CO2, H2O, and N2) is high enough only in a very narrow range of A/F around its stoichiometric value. Therefore, a closed-loop control is necessary to maintain the correct stoichiometric A/F ratio [2].

Fig. 1 presents a simplified block diagram of the control loop employing a sensor of the oxygen content in exhaust gases.

An oxygen (or lambda) sensor is an electrochemical cell capable of detecting the oxygen content of exhaust gases [3], [4]. Fig. 2 shows the schematic cross-section of a typical lambda sensor. The sensor is mounted in the exhaust manifold of a vehicle in such a way that one of the two electrodes is in contact with the exhaust gases while the other is in contact with the atmosphere. The sensor produces a voltage which shows a logarithmic dependence on the ratio of the equilibrium oxygen contents in the atmosphere and in the exhaust gases.

The sensor output voltage $V_o$ as a function of $\lambda$ is shown schematically in Fig. 3. The output signal lies in a range smaller than 1 V, and displays a sharp voltage jump whenever $\lambda$ crosses value 1, thereby indicating whether the mixture is richer or leaner than the stoichiometric value. As a result, the sensor signal is nearly a step function around the stoichiometric A/F ratio. Another important parameter of the oxygen sensor is the temperature, since the response time of the lambda sensor $T_r$ depends heavily on it [3], [5]. When the device is operated

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L. Civardi is with Italei—the SIT, Castelletto di Sotto Milanese, Milano, Italy.
U. Gatti, F. Maloberti, and G. Torelli are with the Department of Electronics, University of Pavia, Pavia, Italy.

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at a higher than 600°C temperature, the response time to a step change in the A/F ratio is less than 100 msec and is less than 300 msec for temperatures as low as 300°C. The temperature also affects the output resistance \( R_o \) of the oxygen sensor. At low temperatures (<300°C), \( R_o \) is greater than 100 kΩ, while it becomes less than 1 kΩ at temperatures higher than 500–600°C [6].

The control loop shown in Fig. 1 includes a central processing unit (CPU) which controls the electronic fuel injectors. In a typical system, the sensor output signal is amplified and is then fed to a comparator. Its output is then processed to obtain the control signal for the injectors. To achieve proper system operation, a precise voltage should be fed to the comparator input when the average A/F ratio of the mixture is equal to stoichiometry. To suit the sensor output signal for feeding into the processing system, a proper electronic interface is required. The interface should provide differential to single-ended conversion with accurate voltage gain and satisfactory linearity. Moreover, the sensor output voltage should be shifted around a proper reference level. The processing system and the oxygen sensor are placed far away from each other, and therefore, they have different ground references. The difference in ground voltages \( V_{\text{GND}} \) in extreme cases may be as large as ±1 V [6]. As a consequence, a good common mode rejection should also be provided by the interface. In particular, the output voltage in the presence of a stochiometric A/F ratio \( V_{\text{GND}} \) should be independent on the input common mode voltage. The interface must also be capable of detecting error conditions such as a short-circuit or open wires in the connection to the sensor. Finally, a very high input resistance should be provided.

This paper presents a CMOS interface developed to meet the above requirements. The use of a conventional CMOS technology instead of a bipolar technology [6] facilitates the integration of the interface in the same chip together with the process unit, thus achieving a very compact system. Moreover, a single 5 V supply is required and a low power consumption is achieved.

The feasibility of the proposed approach has been demonstrated previously [7]. However, some features were not included such as the detection of error conditions and the compensation of nonideal effects which lead to a degradation in the conversion linearity and in the common mode rejection, as will be described later.

The complete block diagram of the developed interface is shown in Fig. 4. The first block (B1) performs the required differential to single-ended conversion and the level shifting of the output voltage around a given reference voltage \( V_r \). This provides a good common mode rejection (CMR) and a fairly accurate voltage gain. \( I_{\text{low-}} \) and \( I_{\text{low-}} \) are microcurrents used to detect the open-wire condition. The second block (B2) amplifies the signal delivered by block B1. The voltage gain required of the interface is obtained with a proper value of the ratio \( R_2/R_1 \). Finally, \( R_r \) and \( C_r \) provide low-pass filtering so as to reject high-frequency noise. A large filtering time constant is required (in the order of 10 ms), which results in large values of either \( R_r \) and/or \( C_r \). These can be implemented using at least one external discrete component or adopting integrated switched-capacitor techniques.

This paper describes the design and the integrated realization of block B1, which is the most critical one, together with its measured performance. The results obtained show that the circuit provides an accurate voltage gain as well as a satisfactory common mode rejection and a good linearity for the above specified signal ranges \( (V_{\text{GND}} = \pm 1 \text{ V}, V_r = 0 \text{ to } 1 \text{ V}) \). The value of \( V_{\text{GND}} \) displays a variation as small as 2 mV over the whole common mode input range, thereby meeting the specifications required.

II. DIFFERENTIAL TO SINGLE-ENDED CONVERTER

This circuit is made up of a transresistance stage followed by a transresistance stage (Fig. 5). The first stage performs the differential to single-ended conversion, delivering a current output signal, \( \Delta I \). The second stage performs the current-to-voltage conversion and the level shift around the reference voltage \( V_R \).

The two input transistors M1 and M2 are identical, and are forced to work in their triode region. The input signal is applied to the gate electrodes of M1 and M2: \( V_{G1} = V_{\text{GND}} + V_s \) and \( V_{G2} = V_{\text{GND}} \). In an initial approximation, the current-voltage characteristic of transistors M1 and M2 operated in the triode region is expressed by [8]:

\[
I_D = \mu C_{\text{ox}}(W/L)V_{DS}(V_{GS} - V_{T}) - \frac{1}{2}V_{DS}^2
\]

where \( I_D \) is the drain current, \( V_{DS} \) and \( V_{GS} \) are the drain-to-source and gate-to-source voltages, \( \mu \) is the effective channel
electron mobility, $C_{ox}$ is the gate oxide capacitance per unit area, $W$ and $L$ are the effective channel width and length, respectively, and $V_{th}$ is the threshold voltage of p-channel transistors, which is assumed to be equal in M1 and M2. Assuming that the drain-to-source voltages of M1 and M2 have the same quiescent value ($V_{DS1} = V_{DS2} = V_{DS}$), and that the difference between $V_{DS1}$ and $V_{DS2}$ in the presence of a differential input signal is negligible, the difference $\Delta I$ between the currents $I_{D2}$ and $I_{D1}$ flowing through transistors M2 and M1 is equal to

$$\Delta I = I_{D2} - I_{D1} = -\mu C_{ox}(W/L)(V_{GS1} - V_{GS2})V_{DS}. \quad (3)$$

Assuming that $V_{DS}$ does not depend on the input signal, $\Delta I$ is proportional to the difference between $V_{GS1}$ and $V_{GS2}$, and therefore, to the differential input signal. It is also independent of the common mode input signal.

Transistors M5, M6, M7, M8 form a cascode current mirror which provides excellent current matching [9], thus allowing us to obtain the output current of the stage as the current difference $\Delta I$.

The current $\Delta I$ is then converted into a voltage by the cascaded transresistance stage. This stage is equivalent to the transconductance stage. The corresponding components of the two stages are identical, therefore, a symmetrical circuit is obtained. When nonidealities are neglected, the transresistance of the second stage is exactly equal to the reciprocal of the transconductance of the first stage, therefore, the overall voltage gain of the two cascaded stages is nearly unit. Taking into account the dependence on the input common mode voltage (Section III), a reduction of the gain in the range of 15% is expected.

The stage made up of transistors M17, M18, M19, and M20 performs the required level shift of the output voltage around the reference voltage $V_R$.

Blocks $A1 \pm A5$ are conventional two-stage operational amplifiers with internal pole-splitting compensation [10]. Amplifiers $A1 \pm A4$ keep the drain-to-source voltages of M1, M2, and M9, M10 equal to $V_{B1}$ and $V_{B1'}$, respectively, independently of the input signal level. Therefore, assuming that $V_{B1}$ and $V_{B1'}$ have a constant adequate value, transistors M1, M2, M9, and M10 work in their triode region with a constant drain-to-source voltage. In the simplest approach, $V_{B1}$ and $V_{B1'}$ are set to a constant value (e.g., $V_{DD} = 0.2$ V). In the next section, it will be shown that the use of appropriate separate bias voltages $V_{B1}$ and $V_{B1'}$ improves the common mode rejection of the circuit. The operational amplifiers were designed to work with the required large input common mode signal.

The open-circuit condition is detected by means of an auxiliary circuit, which feeds a constant microcurrent $I_{low}$ into the wires leading to the sensor (Fig. 4). When the connection between the sensor and the inverting input is open, the inverting input of the interface is forced to a higher level, thereby forcing the output voltage to a lower level. On the contrary, a high output level is forced in case of a broken connection between the sensor and the noninverting input. In both cases, the control processing unit detects the interface output voltage and reveals the incorrect operation. The short-circuit condition forces the output voltage of the circuit to $V_R$.

After sensing the presence of this voltage for a predetermined time interval, the control processing unit then detects the faulty condition.

The amplifier A5 is included in a feedback loop which sets the quiescent interface output voltage at $V_R$. This feedback loop also keeps the voltage at node $N$ equal to $V_{IH}$. This value is set equal to the nominal value of the voltages at nodes 1 and 1'. This ensures the best operation of the cascode current mirrors in the transconductance and the transresistance stages.

Finally, it is clearly seen that the proposed structure shows a very high input resistance.

III. ANALYSIS OF NONIDEALITIES

A more accurate analysis of the circuit requires taking into account the dependence of the effective channel electron mobility $\mu$ on the gate-to-source voltage $V_{GS}$. Equation (2) becomes

$$I_D = \frac{\mu_0}{1 + \theta [(V_{GS} - V_{Tn})]} \cdot C_{ox}(W/L)V_{DS}[(V_{GS} - V_{Tn}) - \frac{1}{2}V_{DS}] \quad (4)$$
where $\mu_0$ is the zero-field carrier mobility and $\theta = \beta_0 l_{ox}$ is the mobility degradation coefficient; $l_{ox}$ is the gate oxide thickness, and $\beta_0$ ranges typically from 0.001 to 0.004 $\mu m V^{-1}$ [8]. From (4), it follows that nonlinearities exist in the relationship between the differential input voltage $V_i$ and the current $\Delta I$ generated by the transconductance stage.

Nonlinearities are dependent on the input common mode voltage. In the proposed circuit, the source electrodes of input transistors M1 and M2 were directly connected to $V_{DD}$ in order to maximize the value of $|V_{GS} - V_{Tr}|$, thereby minimizing the variation of the effective channel electron mobility in the presence of an applied input signal. Let us consider first the dependence of the circuit behavior on the input common mode voltage $V_{AGND}$, assuming a differential sensor signal $V_s \ll |V_{AGND} - V_{DD} - V_{Tr}|$. The currents through transistors M1 and M2 are approximately given by:

$$I_{D1} = K_0 I_{DS}[V_{AGND} - V_{DD} - V_{Tr} - \frac{1}{2} V_{DS} + V_s]$$

$$I_{D2} = K_0 I_{DS}[V_{AGND} - V_{DD} - V_{Tr} - \frac{1}{2} V_{DS}]$$

where

$$K_0 = \frac{W/L}{1 + \theta (|V_{AGND} - V_{DD} - V_{Tr}|)} C_{ox} \mu_0$$

The current difference $\Delta I = I_{D2} - I_{D1}$ results equal to

$$\Delta I = -K_0 V_{DS} V_s.$$  

(6)

Therefore, the current $\Delta I$ delivered by the transconductance stage in the presence of a given differential sensor signal shows some dependence on the input common mode voltage $V_{AGND}$. On the other hand, when performing the conversion of current $\Delta I$ into a voltage, the transresistance stage does not introduce any additional term dependent on the input common mode voltage, as the quiescent output voltage of the circuit is set at $V_R$ regardless of the value of $V_{AGND}$. Thus, assuming that the voltage gain of the two level shifters (transistors M17, M18 and M19, M20, respectively) is equal to unit, we can write

$$V_{out} = V_R - \frac{\Delta I}{K_0 V_{DS}} = V_R + \frac{\mu_0}{K_0 V_{DS}} V_s.$$  

(7)

where $V_{DS}$ is the drain-to-source voltage of transistors M9 and M10, and

$$K_0' = \frac{(W/L)}{1 + \theta (|V_R - V_{Tr} - V_{oM20} - V_{DD} - V_{Tr}|)} C_{ox} \mu_0.$$)

$V_{Tr}$ is the threshold voltage of n-channel transistors, and $V_{oM20}$ is the overdrive voltage of transistor M20. It is worth pointing out that $K_0'$ is independent of the input common mode voltage.

Therefore, the dependence of the converter output voltage on $V_{AGND}$ is due only to the transconductance stage. From (6) and (7), for a 3-um process with $\theta = 0.055 V^{-1}$ and $V_{Tr} = -1 V$, the variation in the current $\Delta I$ and, hence, in the voltage $V_{out}$, is expected to be about 9% when $V_{AGND}$ ranges from -1 V to 1 V in the presence of a nonzero input differential signal. This behavior introduces a degradation in the common mode rejection of the circuit. To improve CMR performance, compensation for the degradation in the channel electron mobility can be accomplished by adjusting the drain-to-source voltage of input transistors M1 and M2 or of transistors M9 and M10, and hence their transconductance as a function of the input common mode voltage. In the circuit proposed, this is obtained by making the bias voltage $V_{B1}$, which sets the drain-to-source voltages of transistors M9 and M10, dependent on the input common mode signal, while keeping $V_{B1}$ constant.

Fig. 6 shows the circuit which generates the bias voltages $V_{B1}$ and $V_{B1}$. The bias voltage $V_{B1}$ is generated by the structure made up of transistors M39, M40, M41 (the former is operated in its triode region and its gate is connected to ground). The nominal value of $V_{B1}$ was set at $V_{DD} - 0.2 V$ by suitably sizing these transistors.

In the circuit which generates the bias voltage $V_{B1}$, transistor M39 is replaced by a differential structure. Both branches of this structure are made up of two series-connected transistors (M48, M50 and M49, M51, respectively), which are operated in their triode region as well. The gate electrodes of transistors M48 and M49 are connected to the input terminals of the interface.
When the input common mode voltage rises, the electron mobility degradation produces an increase in the output current of the transconductance stage \( \Delta I \) for any given nonzero input differential voltage, while \( K_c \) increases. Since the same input signal is also fed to the gates of transistors M48 and M49, the voltage \( V_{B1} \) is reduced, thus producing an increase in the drain-to-source voltage \( V_{DS} \) of transistors M9 and M10. When these two opposite effects are made approximately equal, the desired compensation is achieved (7). By choosing suitable sizes of transistors M48, M49, M50, and M51, an adjustment of about 12 mV is obtained in \( V_{B1} \) over an input common mode voltage range of 2 V. Indeed, because of the differential topology of the mobility degradation compensation circuit, an input differential signal does not substantially affect the value of voltage \( V_{B1} \).

The behavior of the circuit when an input differential signal is applied will now be briefly considered. By expanding the fractional term in (4) in a Taylor series with respect to \( V_{DS} - V_T \), around the quiescent point \( (V_{AGND} = V_{DD} = V_T) \), an expression containing even- and odd-order nonlinear terms is obtained for current \( I_D \). The second-order nonlinear term is dominant. However, due to the differential circuit topology, the current \( \Delta I \), as defined by (3), contains only odd-order nonlinear terms; in particular, third-order nonlinearities become the dominant ones. Of course, when \( V \) is applied, a common mode component also results. With the above value of \( \theta \) and with the worst-case value of \( V_{AGND} \) (1 V), a variation as small as fractions of 1% is expected in the value of the transconductance of the first stage over an input differential voltage range equal to 1 V.

The analysis of the nonlinearities introduced by the transresistance stage is similar. It can be observed that while the gate-to-source voltage of M10 changes as a function of current \( \Delta I \), the gate-to-source voltage of M9 is kept constant. Thus, both even and odd-order nonlinear terms are introduced into the output voltage of the stage when current \( \Delta I \) is injected. In particular, the second-order term is the dominant one, and a variation of about \( \approx 10\% \) in the value of \( g_m \) is to be expected over the specified input voltage range with the above process parameters.

In practice, the dominant nonlinearities introduced by the differential to single-ended converter when a differential input signal is applied, are due to the terms contributed by the transresistance stage. The resulting linearity is satisfactory for the intended application.

The circuit shown in Fig. 6 also generates the microcurrents \( I_{out+} \) and \( I_{out-} \) used to detect open-wire conditions. These microcurrents are obtained as scaled-down replica of the reference current \( I_{ref} \). Their value was set at \( \approx 2\mu A \), thereby producing a negligible voltage drop on the sensor output resistance and on the ground connection resistance during correct operation.

**IV. MEASURED PERFORMANCE**

The proposed interface circuit was designed and optimized using the PRECISE simulation program [11], and was then integrated in a conventional 3-\( \mu \)m single-metal double-polysilicon p-well CMOS technology. The active area of the integrated test chip (Fig. 7) was about 2.4 \( \text{mm}^2 \).

The power supply voltage was \( +15 \) V, while the reference voltage \( V_{R} \) was set at 2.5 V. The current \( I_{ref} \) and the voltage \( V_{D2} \) was set equal to 10 \( \mu A \) and to 2 V, respectively. The measured quiescent current consumption of the circuit was 220 \( \mu A \) under the worst-case value of \( V_{AGND} \) (1 V).

The measured transfer characteristic of the converter, \( V_{out} \) vs \( V_{in} \), is shown in Fig. 8 (\( V_{AGND} = 1 \) V). The resulting small-signal voltage gain (\( \text{Gain} = \delta V_{out}/\delta V_{in} \)) as a function of the differential input voltage \( V_{in} \) is shown in Fig. 9. The voltage gain is equal to 0.88 with an overall variation of about \( \pm 6.5\% \) over an input differential voltage range of 1 V. These results generally coincide with theoretical analyses of circuit nonlinearities.

Fig. 10 shows the transfer characteristics of the circuit when a common mode voltage \( V_{AGND} \) of \( -1 \) V and 1 V, respectively, is superimposed on an input signal \( V_{in} \) ranging from 0 to 1 V. As expected, the transfer characteristics show some dependence on the input common mode voltage. The resulting large-signal voltage gain varies from 0.80 when \( V_{AGND} \) is \( -1 \) V to 0.88 when \( V_{AGND} \) is 1 V (the variation
V. CONCLUSIONS

The control of the A/F ratio in modern engines is a key factor in the reduction of automotive pollution. It can be performed by means of a feedback loop employing a three-way catalytic converter, a lambda sensor, a control processing unit, and electronic fuel injectors.

This paper has presented a novel CMOS interface which prepares the sensor output signal to be fed to the central processing unit. The integrated interface provides differential to single-ended conversion with good common mode rejection, accurate voltage gain, and satisfactory linearity. The measured performance meets the specifications required for automotive applications.

REFERENCES


Lorenzo Civardi was born in Pavia, Italy, in 1963. He graduated in 1990 with the Laurea degree in electronics engineering from the University of Pavia, Pavia, Italy. In 1991, he joined Italtel-SIT Design Center, Milano, Italy. His present interests are in the field of CAD for integrated circuits, particularly, he is concerned with the development of macromodels for analog simulators.

Umberto Gatti (S'90) was born in Pavia, Italy, in 1962. He received the Laurea degree in electronics engineering summa cum laude in 1987 from the University of Pavia, Pavia, Italy. In 1988, he joined the Department of Electronics of the same university, where he is currently working towards the Ph.D. degree in electronics and information engineering. His research interests are in the area of CMOS integrated circuits for analog signal processing. At present he is involved in the design of continuoustime filters and high-speed data converters.
Franco Maloberti (S'87) received the Laurea degree in physics _summa cum laude_ in 1968 from the University of Parma, Parma, Italy. He joined the University of L'Aquila in 1968 and the University of Pavia in 1969. Currently, he is Full Professor of Design of Components and Integrated Circuits at the University of Pavia. His professional expertise concerns the design and the characterization of integrated circuits for analog applications. He has designed numerous integrated circuits applying innovative solutions. Some of these designs were for commercial telecommunication applications requiring high-speed analog signal processing, D/A and A/D circuitry, and were implemented in CMOS and JFET-CMOS technologies.

Dr. Maloberti has authored/coauthored more than 100 papers and holds 11 patents. He was awarded for the XIII G. Pedriali Prize in 1990. He is a Member of AEI (1983).

Guido Torelli (M’90) was born in Roma in 1949. He received the degree in electronic engineering with honors, from the University of Pavia, in 1973, where, after graduating, he worked one year in the Institute of Electronics on a scholarship. In 1974 he joined SGS-ATES (now SGS-Thomson Microelectronics), where he served as a design engineer for MOS ICs, involved in both digital and analog circuit development, and where he became responsible for the design group of MOS ICs for consumer applications. In 1987 he joined the Department of Electronics of the University of Pavia as an Associate Professor of Electronics Materials and Technologies. His research interests are in the area of MOS integrated circuit design. At present, he is mainly concerned in the fields of CMOS analog circuits and analog/digital interfaces. He is a Member of AEI.