CMOS triode-transistor transconductor for
high-frequency continuous-time filters

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Abstract: The paper describes a high-frequency fully-CMOS differential transconductor, which uses MOS transistors biased in the triode region with a constant drain-to-source voltage. The measured total harmonic distortion (THD) of the transconductor achieved using conventional 2 μm n-well CMOS technology, is −46 dB for a 12V peak
input signal at 10 MHz (supply voltage = 5 V). A second-order continuous-time filter with the
characteristic frequency tunable in the 10 MHz range is realised. It occupies a silicon area of 0.21 mm²
and requires a power consumption of 12 mW. Its measured THD (in the low-pass configuration) is
−50 dB with a 0.8V peak differential input. Tuning capabilities are also shown.

1 Introduction

The integration of high-frequency filtering functions with conventional CMOS processes allows the implementation of mixed systems on a single chip for applications such as digital television and hard-disk drives. For this purpose, continuous-time filtering techniques have been successfully developed.

Two basic topologies were proposed: MOSFET-C [1–3] and g_m-C [4–7]. The first approach uses transistors in the triode region, operational amplifiers (OAs) and capacitors. It suffers from limitations under high-frequency operation deriving from the OAs, as its gain-bandwidth product must be much higher than the operating frequency of the filter [8–10]. One way to overcome this problem is to use BiCMOS technologies to realise high-frequency OAs [11, 12]. However, this leads to a cost increase.

The second approach uses integrators based on transconductors and capacitors. In this case, the second pole of the same transconductors limits frequency performance [13]. However, by employing simple architectures, this pole can be set at a very high frequency, making g_m-C the preferred technique for high-frequency filtering applications [14], such as luminance filters for conventional television, anti-aliasing filters for digital television, noise-rejecting filters for hard-disk drives, etc.

Transconductors for CMOS g_m-C filters can be implemented in different ways, including the use of a differential stage with MOS transistors in saturation [15–22]; the use of MOS transistors in the triode region [23–25]; and the use of both a differential stage and a MOS transistor in triode with \( V_{ds} \approx 0 \) V [26–28]. In the approach using differential stages, transconductance linearity is confined to a small input range, so that, for a large input swing, additional complex linearising circuitry is necessary. In this manner, a very good performance has been obtained [17, 20]. On the other hand, use of transistors in the triode region permits simpler realisation at potentially higher speeds while allowing conventional CMOS technology to be used [29]. Realisations based on MOS transistors in triode using BiCMOS technology [30–32] are very attractive for high-frequency applications. However, the ensuing fabrication-cost increase can be a major drawback in a number of large-volume applications, where the use of conventional CMOS processes is strongly preferred.

This paper presents a 2 μm fully CMOS implementation of a novel transconductor based on the triode-transistor approach. A biquadratic cell using the proposed transconductor is also described. Measurements on integrated structures have proved the effectiveness of this approach for operation frequencies higher than 10 MHz. Moreover, the range of tunability attained allows us to compensate for process parameter spreads in automatically tuned filters. Measured linearity, with its great flexibility and simplicity, makes this transconductor very well suited to high-frequency filtering applications.

2 Transconductor topology

The proposed differential transconductor is shown schematically in Fig. 1 [33]. It is derived from a former circuit [29] that shows good performance, but gives lower speed owing to the output current mirrors and that requires more complex control on the current in the output section. The circuit presented includes three basic blocks: a differential cascode transconductor (DCT), a feedback loop (FL) and a common-mode voltage reference (CMR). The DCT is based on two identical input MOS transistors, \( M_1 \) and \( M_2 \), operated in the triode region with a constant drain-to-source voltage. Their signal drain currents are transferred to the output
through M3 and M4, whose gates are controlled by the FL.

At first approximation, the drain currents \( I_d \) of M1 and M2 are given by

\[
I_d = \frac{(W/L)\mu C_{ox}}{V_{th}} \left[ V_{GS} - V_T - \frac{1}{2} V_{DD} \right]
\]

(1)

where the meaning of the symbols is clear \((i = 1, 2)\). If the voltages \( V_{in} \) are kept constant, the drain currents are linear functions of the applied gate-to-source voltages, thus giving rise to a linear transconductance function.

![Fig. 1 Simplified diagram of differential transistor](image)

The drain voltages of M1 and M2, \( V_{D1} \) and \( V_{D2} \), are controlled by the FL. Circuit CMR generates the common-mode level \( V_{CM} \) required for \( V_{D1} \) and \( V_{D2} \). It also generates its shifted version \( V_{CM} \) by means of \( D1, V_{D1} \), and \( V_{D2} \) are shifted upwards by means of \( D2, D3 \), to obtain \( V_{D1} \) and \( V_{D2} \). These are applied to the differential inputs of the three-input OA A, whose outputs control the gates of M3 and M4 in feedback; therefore the differential input of the OA \((V_{in1} - V_{in2})\) is forced to zero, as is the difference between its common-mode value and \( V_{CM} \). This stabilizes both the differential and the common-mode components of \( V_{in1} \) and \( V_{in2} \).

In the circuit CMR, M1 is pushed into the triode region by appropriate choice of its aspect ratio and bias current \((I_b + I_c)\). The structure M1-D1 is matched to the branches M2-D2, and the input transistors M1 and M2 are also kept in triode. The bias current through M1, which equals the one running through M1 and M2, determines \( V_{CM} \) for a given nominal input quiescent voltage \( V_{in0} \). On changing \( I_b \), \( V_{CM} \) and, hence, \( V_{D1} \) and \( V_{D2} \) vary accordingly. Of course, the driving circuit connected to the transconductor inputs must provide a suitable input common-mode voltage level \( V_{in0} \).

An additional benefit of the FL is the increase in the output impedance of cascode structures \( M_{1-}M_{3} \) and \( M_{2-}M_{4} \).

The output signal current of the transconductor \( I_{out} \) is given by

\[
I_{out} = I_{in1} - I_{in2} = g_{m1} V_{in1} - g_{m2} V_{in2}
\]

(2)

where \( V_{in1} \) and \( V_{in2} \) are the signal components of the input voltages \( V_{in} = V_{in1} + V_{in2} \); the transconductances \( g_{m} \) \((i = 1, 2)\) are equal to

\[
g_{m_i} = \frac{g_m}{v_{GS_i}} = \frac{\mu C_{ox}(W/L)}{V_{DD}}
\]

(3)

As \( V_{in1} = V_{in2} = V_{in} \), we have \( g_{m1} = g_{m2} = g_{m} \) and therefore \( I_{out} = g_{m} V_{in} \). The value of \( g_{m} \) depends on \( V_{in0} \), which can be calculated as

\[
V_{in0} = V_{in} - V_T - \sqrt{\left[ (V_{in} - V_T)^2 - 2(1 + I_d)/(\mu C_{ox}(W/L)) \right]}
\]

(4)

Therefore it is possible to tune the transconductance by varying \( I_d \). An equivalent tuning effect is also achieved by controlling \( J_{2} \). However, this control is not practical as it affects the frequency response of the DCT, changing both its output impedance and its pole frequencies. This can give undesired phase contributions to integrators based on this structure. The values of \( W/L \), \( I_1 \) and \( I_2 \) must be chosen so that \( M_1 \) and, hence, \( M_1 \) and \( M_2 \) operate in triode.

Fig. 2 presents the complete circuit diagram of the transconductor. Diodes \( D_2, D_3 \) and \( D_4 \) are realised with

![Fig. 2 Complete diagram of differential transistor](image)

\( M_{11}, M_{12}, \) and \( M_{13}, \) respectively. The current sources \( I_2 \) are implemented by cascode structures \( (M_{1-}M_{3}) \) and \( (M_{2-}M_{4}) \). A common-mode feedback circuit based on triode-operated transistors, \( M_{C1-}M_{C3} \), stabilises the common-mode output voltage. The OA A includes a differential pair \((M_{A1}, M_{A2})\) with active loads \((M_{A3}, M_{A4})\).

To implement the required common-mode feedback of the control loop, a third branch was added \((M_{A5}, M_{A6})\). \( M_{A5} \) helps to reduce the systematic offset in the loop.

The frequency performance of the transconductor is determined by its second pole. Its frequency is approximately equal to \( f_2 \approx \left[ g_m (A_{21} + 1) + g_{m1}/\left(2\pi C_{ox}A_{23} + 1 + C_{D1}\right)\right] \), where \( C_{D1} \) is the total parasitic capacitance at the drain of \( M_1 \) and \( A_{23} \) is the differential gain of the three-input OA at \( f_2 \). \( f_2 \approx 200 \text{ MHz} \), based on simulations for a conventional 2 µm CMOS process. We connected two feedforward capacitors \( C_{D1} \) and \( C_{A2} \) between the transconductor inputs and the gates of \( M_3 \) and \( M_4 \), thereby introducing a zero at a frequency \( f_z \approx \left[ g_{m1}/\left(2\pi C_{ox} + 1\right)\right]/\left(2\pi C_{D1}\right) \), where \( z = V_{in0}/V_{in} \) and \( A_{23} \) is the differential gain of the three-input OA at \( f_z \). This is made nominally equal to \( f_2 \), thus reducing the effect of the second pole.

The benefit of this solution is demonstrated by Fig. 3 \((C_{A1} = C_{A2} \approx 0.2 \text{ pF})\). The frequency range where deviation from the ideal 90° phase shift is maintained to within \( \pm 1 \) is thereby extended from 5 to 35 MHz. Of course, the benefits of this feedforward compensation are limited by changes in the process parameters. However, simulations have shown that, in the worst case, the operating range still extends up to 22 MHz. \( C_{A1} \) and \( C_{A2} \) also perform the frequency compensation of the feedback loop.

Eqn. 3 shows that the transconductance is constant for any given \( V_{in0} \). However, if the dependence of the carrier mobility \( \mu \) on the gate-to-source voltage \( [34] \) is taken into account, the output current (eqn. 2) becomes

\[
I_{out} = 2g_m (I_d (v_{in2}^2) + a_1 (v_{in2}^4) + \cdots)
\]

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where \( a_1 \approx 1, a_2 = \theta^2 \left( 1 + \theta(V_{m0} - V_p) \right) \) (\( \theta \) is the mobility degradation coefficient, which is inversely proportional to the gate oxide thickness). In eqn. 5, even-order nonlinearities are cancelled by the fully differential topology. The resulting nonlinearity in the transfer characteristic is dominated by the third term, and the deviation of \( g_m \) from linearity is given by [19]

\[
NL_3[\%] \approx \frac{3}{4} \frac{a_2}{a_1} (V_m)^2 \times 100
\]

\[
= \frac{3}{4} \left( 1 + \theta(V_{m0} - V_p) \right)^2 (V_m)^2 \times 100
\]

(6)

where \( V_m \) is the input signal range. For a sinusoidal input with amplitude \( V_m \), \( THD \) is substantially equal to the third-order harmonic distortion \( HD_3 \) [35]:

\[
THD \approx HD_3 \approx \frac{1}{4} \frac{a_2}{a_1} (V_m)^2
\]

(7)

The value of \( \theta \) sets an upper theoretical limit to the achievable linearity. A typical value of \( \theta \) for a conventional 2 \( \mu \)m n-well CMOS technology is 0.09 V\(^{-1}\); therefore, for \( (V_{m0} - V_p) = 1.65 \) V, \( a_2/a_1 \) is 0.006 V\(^{-2}\). For a sinusoidal input signal with a 0.8 V and 1.6 V peak amplitude, a \( THD \) of about 0.096% (\( \approx -60 \) dB) and 0.399% (\( \approx -48 \) dB), respectively, is to be expected.

3 Filter implementation

Any active filter implementation requires basic functions such as integration, lossy integration and addition. With a \( g_m \) filter, the addition is achieved by simply connecting the output of the transconductors that deliver the signals to be summed. The current obtained is fed to a capacitor or to the parallel connection of a capacitor and a resistor, to perform either the integration or the lossy integration, respectively. However, when a voltage signal must be used a given number of times, it must be converted into a current by an equal number of transconductors. To give an example, for the leap-frog flow diagram in Fig. 4a, the state variable \( V \) must be transformed into a current twice (Fig. 4b) to obtain the two integrations. Thus, the number of transconductors required is twice the number of integrations. As suggested in References 21 and 36, this limit can be overcome if the addition (or the subtraction) of voltages is performed at

![Fig. 3 Simulated phase characteristic of an integrator based on the proposed transconductor with and without feedforward capacitors
a With feedforward capacitors
b Without feedforward capacitors](image)

![Fig. 4 Example of a leap-frog section
a Signal flow graph
b Realisation with conventional single-input transconductors
c Realisation with double-input transconductors](image)

![Fig. 5 Four-input version of DCT
FL
I1
I2
M1
M2
M3
M4
C_{BL}
C_{BL}
C_{BL}
C_{BL}
C_{BL}
in
in
in
in
out
out
out
out
V_{SS}
V_{m0}](image)
The practical use of the proposed transconductor was demonstrated by means of the fully differential biquadratic cell shown in Fig. 6 [37], where $C_p$ represents the parasitic output capacitance of the transconductors. Only two transconductors are necessary. The cell provides multiple transfer functions: lowpass, bandpass, highpass and notch. If the two transconductors are identical, the transfer function of the filter in its bandpass configuration is

$$H_{np}(s) = \frac{s(g_{m}/C)}{s^2 + s(g_{m}/C) + (g_{m}/C)^2}$$

(8)

The nominal value of the characteristic frequency $\omega_{np}$ is equal to $g_{m}/C$. The nominal value of the quality factor $Q_p$ is unity [37].

The frequency response of the cell is affected by non-idealities such as the finite output resistance $R_o$ and the parasitic output capacitance $C_p$ of the transconductors [5, 38]. For the specific architecture, assuming $R_o$ and $C_p$ equal for both integrators, the real characteristic frequency $\omega_{np}$ is

$$\omega_{np} = \omega_{0n} \frac{C}{C_p + C} \sqrt{1 + \frac{1}{g_{m}R_o} \left(1 + \frac{1}{g_{m}R_o}\right)}$$

(9)

The real quality factor $Q_p$ is equal to

$$Q_p = \frac{1}{1 + Q^2/(g_{m}R_o)}$$

(10)

If the equivalent gain $g_{m}R_o$ is large enough (>100), the characteristic frequency is affected only by the parasitic capacitance $C_p$:

$$\omega_{np} \approx \omega_{0n} \frac{C}{C + C_p} = \frac{g_{m}C}{C + C_p} = \frac{g_{m}}{C + C_p}$$

(11)

4 Measurements

The transconductor and filter described were integrated using conventional 2 $\mu$m double-poly silicon double-metal n-well CMOS technology (active area: $\approx 0.09$ $mm^2$ and $\approx 0.21$ $mm^2$, respectively). A single CMR block was used for the filter. Fig. 7 shows the microphotograph of the filter.

The current $I_2$ used in the experimental set-up was 200 $\mu$A, and the supply voltage was 5 $V$. Unless otherwise specified, $I_1$ was 100 $\mu$A.

Fig. 8a shows the transconductor voltage-to-current transfer characteristic as a function of the differential input voltage $V_{DIFF}$. The corresponding transconduction is shown in Fig. 8b. The transfer characteristic is linear within 5% for $V_{DIFF}$ ranging from $-1.6$ $V$ to $+1.6$ $V$. As expected, the third-order nonlinearity is the dominant one. The measured value of nonlinearity is in very good agreement with its theoretical value: from eqn. 6, for an input range equal to 3.2 $V$, with $V_{diff} = V_2 -}$

1.65 $V$, we obtain $N_{L} \approx 4.7\%$. The linearity performance of the transconductor was substantially independent of the value of the tuning current $I_1$.

Fig. 7 Microphotograph of the integrated filter

Fig. 8 Transconductor characteristics

a Measured voltage-to-current transfer characteristic ($I_1 = 100 \mu A$, $I_2 = 200 \mu A$, supply voltage $= 5 V$)

b Measured transconductance value

Fig. 9 shows the THD of the transconductor as a function of the sinusoidal input peak amplitude $V_p$ for $f_m = 100$ kHz and $f_s = 5$ MHz. The input signal is applied to the transconductor using a low-impedance sinewave generator and a balanced transformer. The output current is converted into a voltage and fed to the spectrum analyser. The THD remains below $-48$ dB for an input differential signal as large as 1.6$V_{peak}$. As was expected, the third-harmonic component is the dominant one at $f_m = 100$ kHz. The harmonic components for $V_m = 400$ m$V_{peak}$ are mainly due to the experimental set-up used.
The output power spectrum of the transconductor with a 10 MHz 1.2 Vpp input signal (Fig. 10) indicates a THD of $\sim -46$ dB; the second-harmonic component becomes dominant. The progressive worsening in linearity performance with increasing frequencies has been ascribed to the fact that, at high frequency, the FL does not provide a perfect stabilisation of the drain voltages of input transistors $M_1$ and $M_2$. The use of a technology with a lower than 2 $\mu$m minimum gate length could extend the frequency range of the loop stabilisation, at the expense of a higher value for $\theta$.

Fig. 11 shows the tunability of the transconductor: $g_m$ varies by a factor of 2 when $I_1$ varies by approximately one order of magnitude. This allows satisfactory control of filter tuning. As can be seen, the tuning characteristics measured are in good agreement with simulation results.

The frequency response of the biquadratic cell in its bandpass configuration is shown in Fig. 12a ($I_1 = 50$ $\mu$A). The poly-to-poly capacitor $C$ used in the cell is 0.7 $\mu$F. As the overall output parasitic capacitor $C_p$ is 0.8 pF, it produces a loss of around $-6.6$ dB in the frequency response owing to the capacitive division of the input signal. Fig. 12b shows the shift of the bandpass frequency response when the tuning current $I_1$ is increased to 100 $\mu$A and 150 $\mu$A: the central frequency moves from 8.4 MHz to 11.6 MHz.

Fig. 13 shows the measured output power spectrum of the filter in its lowpass configuration (500 kHz, 0.8$V_{\text{peak}}$).

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input signal; corner frequency \( f_c = 10 \text{ MHz} \). As expected, the THD, which is mainly contributed by the third-order harmonic component, is below \(-50 \text{ dB}\). It still remains below \(-42 \text{ dB}\) for a differential input peak amplitude of 1 V (Fig. 14).

The PSRR for \( V_{DD} \) and \( V_{SS} \) shows a peak of \(-42 \text{ dB} \) and \(-43 \text{ dB} \), respectively, at a frequency of around 10 MHz (filter corner frequency = 10 MHz), whereas it is much lower over the rest of the frequency range.

The output noise integrated over the band 1–30 MHz is around 600 \( \mu \text{V}_{\text{rms}} \), which is comparable to that of other CMOS realisations [20, 21]. When referred to the maximum input signal amplitude, which causes a less than \(-42 \text{ dB} (1V_{\text{peak}})\) THD, this gives a dynamic range of \(-62 \text{ dB} \).

The power dissipation of the filter is as low as 12 mW \( (f_0 = 10 \text{ MHz}) \).

5 Conclusions

A fully CMOS differential transconductor suitable for high-frequency continuous-time filtering has been described. A transconductor cell and a biquadratic filter with the characteristic frequency tunable in the 10 MHz range were integrated using conventional 2 \( \mu \text{m} \) n-well CMOS technology. The measured THD of the transconductor is \(-46 \text{ dB} \), with a 10 MHz 1.2\( \text{V}_{\text{peak}} \) differential input signal (supply voltage = 5 V). The dynamic range of the filter is \(-62 \text{ dB} \), with THD < \(-42 \text{ dB} \). The silicon area of the filter is 0.21 mm\(^2\), and its power consumption is 12 mW \( (f_0 = 10 \text{ MHz}) \). The performance obtained makes the transconductor proposed suitable for implementing the high-frequency continuous-time filters required in applications such as analogue and digital television, personal computing and intermediate frequency for FM modulators.

6 References


