polarisations the measured value was 2.6 and for the circular polarisation the gain was 2.5. Applying the method presented by Wu *et al.* [9], the unloaded Q-factors Q_0 for the linear and circular polarisations were measured to be 33.8 and 32.0, respectively, and hence the impedance bandwidths are 2.8% and 3.0%, respectively, for a VSWR $\leq$ 2.5. Finally, the Wheeler Cap method [10] was applied to measure the radiation efficiency of the DRA, using a metallic box of 25 (height) $\times$ 50 (width) $\times$ 50 (length) mm^3. The estimated value of the radiation efficiency was 85%. The slightly lower antenna gain, impedance bandwidth and radiation efficiency of the switchable antenna, compared with the corresponding values reported by Drossos *et al.* [5] for a circular polarised DRA, are believed to be due to the more complex feeding circuit used for the switchable DRA. All the results for the switchable DRA are presented in Table 2.

Conclusions: A switchable cylindrical DRA has been reported. The antenna provided linear polarised radiation in two orthogonal planes, circular polarised radiation, or no radiation at all. The experimental results showed that the antenna can provide very good linear and circular polarisation, indicating that the switching-feed circuit was working very effectively. The simple feeding arrangement and antenna structure, the small axial ratio, the large impedance bandwidth and the high radiation efficiency signified the main advantages of the switchable DRA in antenna switching applications.

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Clock feedthrough compensation with phase slope control in SC circuits

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Indexing terms: Switched current circuits, Analogue circuits

A clock feedthrough compensation technique for SC circuits is presented. The principle is based on the control of the switch turn-off slope. A single control block can drive a large number of identical SC structures, thus minimising area overhead. Experimental results from an integrated prototype show that the injected charge is reduced by a factor as high as 13.

Introduction: Clock feedthrough due to MOS switches turning off [1] is a major limitation in switched capacitor (SC) circuits because it causes voltage errors intolerable for very accurate applications. The use of complementary and dummy switches [2] alleviates this problem, but the residual error may still be too large. Fully differential topologies [3] greatly help, but at the cost of a considerable increase in silicon area. More sophisticated solutions can also be adopted, such as connecting a suitable SC injecting structure to the op-amp noninverting input [4], using feedback techniques [5], adding auxiliary inputs to the op-amp [6] or feedthrough charge storage capacitors [7].

This Letter presents a novel clock feedthrough compensation technique. The turn-off rate in complementary switches is controlled to minimise the net injected charge over a whole clock cycle. A complex system including a large number of identical SC structures requires only one control block, minimising area overhead. Examples are pipeline analogue/digital converters (ADCs) or banks of algorithmic ADCs used to convert the signal delivered by a sensor array [8], where area requirements are of utmost importance because the pitch of the ADC must fit that of the sensor array.

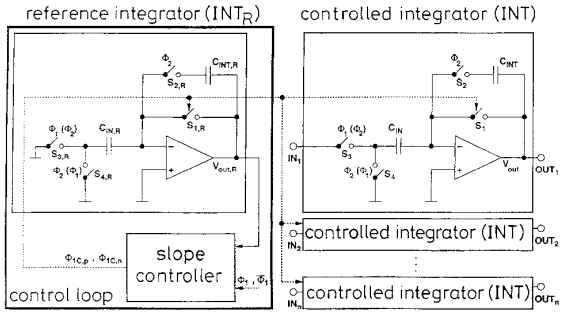

Fig. 1 *Complete circuit for proposed structure for charge injection compensation*

Φ_1 and Φ_2 are nonoverlapping clock phases

Proposed compensation technique: Let us consider the specific SC topology shown on the right in Fig. 1. It is a stray insensitive integrator (INT), which delivers a valid output during Φ_2. The topology used prevents the integration of the op-amp offset [9], but not the integration of the charge injected by S_1 and S_2, as is typical for SC integrators. These two switches are realised, as usual for SC circuits, by two complementary transistors.

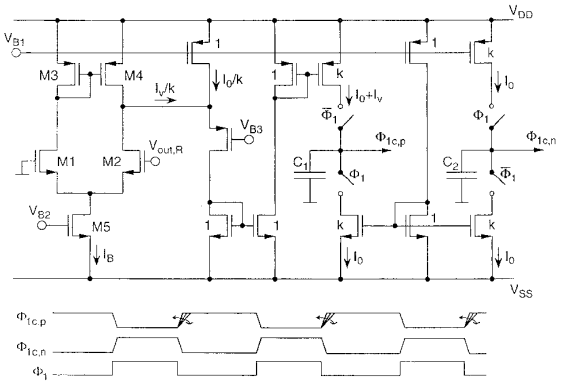

Fig. 2 *Detailed schematic diagram of slope controller*

The net feedthrough charge on C_{INT} observed at Φ_2 and collected during an entire clock cycle (Φ_1 + Φ_2) derives from switching on S_2 ($Q_{2,on}$), switching it off previously ($Q_{2,off}$) and switching off S_1 ($Q_{1,off}$). To obtain perfect compensation, we must have

$$Q_{1,off} = -Q_{2,off} - Q_{2,on} \quad (1)$$

We achieve this result by exploiting the dependence of charge injection on the switch turn-off rate [1]. Specifically, in our circuit we adjust the turn-off slope of the phase driving the p-channel device in S_1 (phase $\Phi_{1c,p}$) using a negative-feedback loop. This

includes a reference integrator (INT_R) identical to those that must be compensated (INT) and driven by the same phases. The reference integrator's input is connected to analogue ground, so that only the charge injected by $S_{1,R}$ and $S_{2,R}$ is integrated on $C_{INT,R}$ and contributes to its output voltage $V_{out,R}$. This, in turn, adjusts the turn-off slope of $\Phi_{1c,p}$ by means of an appropriate circuit ('Slope controller') until eqn. 1 is satisfied.

After a transient $V_{out,R}$ reaches a stable value, meaning that the clock feedthrough charge becomes zero. Since the physical structures of INT and INT_R are identical and corresponding switches are driven by the same phases, the net charge injected by S_1 and S_2 also goes ideally to zero.

Phase slope controller: The driving phases of S_1, $\Phi_{1c,p}$ and $\Phi_{1c,n}$ are derived from Φ_1 using the circuit in Fig. 2. The edge slopes of the two phases depend on the charging/discharging currents of capacitors C_1 and C_2 ($C_1 = C_2$). A constant current I_0 determines the fixed slope, S_0, of both edges of $\Phi_{1c,n}$ and the turn-on edge of $\Phi_{1c,p}$. The turn-off slope of $\Phi_{1c,p}$, $S_{off1,p}$, is obtained by adding a variable current I_V to I_0. The variable current is the output of the differential transconductance stage (M_1 to M_5) suitably scaled by a factor of k. By inspection of the circuit we obtain

$$S_{off1,p} = S_0 - \frac{k\sqrt{\mu_n C_{ox}(W/L)_{M1} I_B}}{C_1} V_{out,R} \qquad (2)$$

The value of C_1 and C_2 is determined on the basis of the load due to all the driven integrators. The sensitivity $\Delta S_{off1,p}/V_{out,R}$ is chosen as the best tradeoff between accuracy in obtaining the slope on one hand and integrator output range and/or differential stage input range on the other. The transient needed to reach the steady state of the compensation loop is not important: we simply assume that the reference integrator is reset only at power-on.

Experimental results: The circuit in Fig. 1, including one controlled integrator, was implemented in a conventional double-metal single-poly implanted-capacitor 1.2μm *n*-well CMOS technology (Fig. 3).

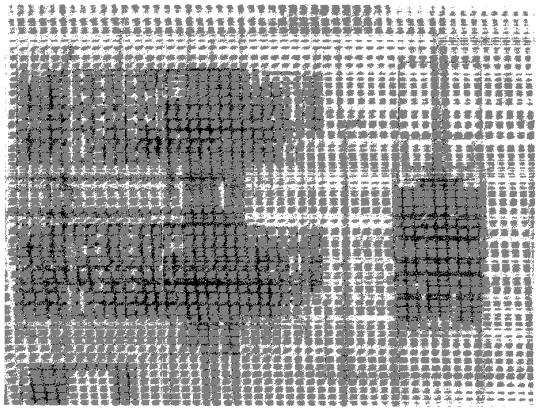

Fig. 3 *Chip microphotograph*

The relatively small value of the integration capacitor (C_{INT} = 0.5pF) allows us to observe charge injection better. Sizing of the transistors in switches $S_1$and S_2 was optimised by computer simulation. The target was to maximise the range of charge injection control, to allow the best mismatch compensation. The constant slope S_0 was set to 0.5V/ns ($C_1 = C_2$ = 5 pF, I_0/k = 100 μA, k = 25). To obtain slope sensitivity$\Delta S_{off1,p}/V_{out,R}$ = ~2×10^9 s^{-1}, we set I_B = 200μA and $(W/L)M_1$ = 20μm/2μm.

Fig. 4 shows the waveforms measured at the output of the reference (track 2) and controlled (track 3) integrators (clock frequency = 500kHz). The control loop is enabled by the trigger pulse shown in track 1. To avoid saturation, we reset the controlled integrator at the beginning of each group of eight clock cycles. This operation leaves some charge trapped in C_{INT}. The effect produces a small constant offset in the valid output of the integrator (Φ_2), that does not affect circuit operation. Note that, before enabling the control loop, the charge injected at each clock cycle produces a staircase voltage at the integrator output. The feedthrough effect

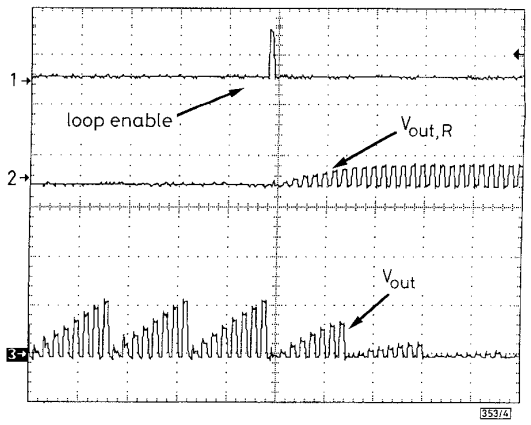

Fig. 4 *Measured waveforms*

1 Trigger pulse (5V/div)
2 Master integrator output (200mV/div)
3 Controlled integrator output (50mV/div)
Horizontal scale: 10μs/div

integrated over eight clock cycles is equal to 60mV, which corresponds to a total charge injection of 120fC (15fC per clock cycle). After the control loop is enabled, $V_{out,R}$ starts to increase and controls the turn-off slope of $\Phi_{1c,p}$. Note that the clock feedthrough effect decreases: it becomes equal to 37mV, 12mV and 5mV for the first, second and third group of clock cycles, respectively. Its steady-state value goes down to 4.6mV, corresponding to a total injected charge of ~9fC (~1.1fC per cycle). This means we reduced the injected charge by a factor of 13.

The residual clock feedthrough is probably due to mismatches between the switches in the reference and controlled integrators. We should also take into account phase shape corruption due to signal propagation. However, since we use rise and fall times as high as 10 ns, this effect is negligible because of integrated circuit size.

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